ABB 5STP04D4200 Control Thyristor datasheet

Patented free-floating silicon technology
Low on-state and switching losses
Designed for traction, energy and industrial applications
Optimum power handling capability
Interdigitated amplifying gate

V_{DRM} = 4200 V
$I_{T(AV)M}$ = 470 A
$I_{T(RMS)}$ = 740 A
I_{TSM} = $7.1 \cdot 10^3$ A
V_{T0} = 1 V
r_T = 1.5 mΩ

Phase Control Thyristor

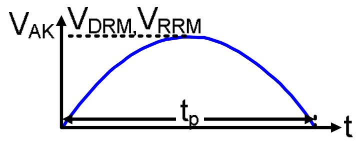
5STP 04D4200

Doc. No. 5SYA1025-07 Nov. 13

- **Patented free-floating silicon technology**
- **Low on-state and switching losses**
- **Designed for traction, energy and industrial applications**
- **Optimum power handling capability**
- **Interdigitated amplifying gate**

Blocking

Maximum rated values [1)]

Parameter	Symbol	Conditions	5STP 04D4200	Unit
Max repetitive peak forward and reverse blocking voltage	V_{DRM}, V_{RRM}	f = 50 Hz, t_p = 10 ms, T_{vj} = 5…125 °C, Note 1 	4200	V
Critical rate of rise of commutating voltage	dv/dt_{crit}	Exp. to $0.67 \cdot V_{DRM}$, T_{vj} = 125 °C	1000	V/µs

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Forward leakage current	I_{DRM}	V_{DRM}, T_{vj} = 125 °C			100	mA
Reverse leakage current	I_{RRM}	V_{RRM}, T_{vj} = 125 °C			100	mA

Note 1: Voltage de-rating factor of 0.11% per °C is applicable for T_{vj} below +5 °C.

Mechanical data

Maximum rated values [1)]

Parameter	Symbol	Conditions	min	typ	max	Unit
Mounting force	F_M		8	10	12	kN
Acceleration	a	Device unclamped			50	m/s^2
Acceleration	a	Device clamped			100	m/s^2

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Weight	m				0.3	kg
Housing thickness	H	F_M = 10 kN, T_a = 25 °C	26		26.6	mm
Surface creepage distance	D_S		25			mm
Air strike distance	D_a		14			mm

1) Maximum rated values indicate limits beyond which damage to the device may occur

On-state

Maximum rated values [1)]

Parameter	Symbol	Conditions	min	typ	max	Unit
Average on-state current	$I_{T(AV)M}$	Half sine wave, Tc = 70 °C			470	A
RMS on-state current	$I_{T(RMS)}$				740	A
Peak non-repetitive surge current	I_{TSM}	t_p = 10 ms, T_{vj} = 125 °C, sine half wave, V_D = V_R= 0 V, after surge			$7.1 \cdot 10^3$	A
Limiting load integral	I^2t				$252 \cdot 10^3$	A^2s
Peak non-repetitive surge current	I_{TSM}	t_p = 10 ms, T_{vj} = 125 °C, sine half wave, V_R= 0.6·V_{RRM}, after surge			$5.9 \cdot 10^3$	A
Limiting load integral	I^2t				$174 \cdot 10^3$	A^2s

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
On-state voltage	V_T	I_T = 500 A, T_{vj} = 125 °C			1.78	V
Threshold voltage	$V_{(T0)}$	I_T = 300 A - 1000 A, T_{vj} = 125 °C			1	V
Slope resistance	r_T				1.5	mΩ
Holding current	I_H	Tvj = 25 °C			75	mA
		Tvj = 125 °C			60	mA
Latching current	I_L	Tvj = 25 °C			500	mA
		Tvj = 125 °C			200	mA

Switching

Maximum rated values [1)]

Parameter	Symbol	Conditions		min	typ	max	Unit
Critical rate of rise of on-state current	di/dt_{crit}	T_{vj} = 125 °C, I_{TRM} = 1500 A, $V_D \leq 0.67 \cdot V_{DRM}$, I_{FG} = 2 A, t_r = 0.5 µs	Cont. f = 50 Hz			100	A/µs
			Cont. f = 1 Hz			1000	A/µs
Circuit-commutated turn-off time	t_q	T_{vj} = 125 °C, I_{TRM} = 2000 A, V_R = 200 V, di_T/dt = -1.5 A/µs, $V_D \leq 0.67 \cdot V_{DRM}$, dv_D/dt = 20 V/µs				600	µs

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Reverse recovery charge	Q_{rr}	T_{vj} = 125 °C, I_{TRM} = 2000 A, V_R = 200 V, di_T/dt = -1.5 A/µs	450		1400	µAs
Reverse recovery current	I_{RM}		25		40	A
Gate turn-on delay time	t_{gd}	T_{vj} = 25 °C, V_D = 0.4·V_{RM}, I_{FG} = 2 A, t_r = 0.5 µs			3	µs

Triggering

Maximum rated values [1)]

Parameter	Symbol	Conditions	min	typ	max	Unit
Peak forward gate voltage	V_{FGM}				12	V
Peak forward gate current	I_{FGM}				10	A
Peak reverse gate voltage	V_{RGM}				10	V
Average gate power loss	$P_{G(AV)}$		see Fig. 7			W

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Gate-trigger voltage	V_{GT}	Tvj = 25 °C			2.6	V
Gate-trigger current	I_{GT}	Tvj = 25 °C			400	mA
Gate non-trigger voltage	V_{GD}	$V_D = 0.4 \cdot V_{DRM}$, T_{vjmax} = 125 °C			0.3	V
Gate non-trigger current	I_{GD}	$V_D = 0.4 \cdot V_{DRM}$, T_{vjmax} = 125 °C			10	mA

Thermal

Maximum rated values [1)]

Parameter	Symbol	Conditions	min	typ	max	Unit
Operating junction temperature range	T_{vj}				125	°C
Storage temperature range	T_{stg}		-40		140	°C

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Thermal resistance junction to case,	$R_{th(j-c)}$	Double-side cooled F_m = 8... 12 kN			36	K/kW
	$R_{th(j-c)A}$	Anode-side cooled F_m = 8... 12 kN			70	K/kW
	$R_{th(j-c)C}$	Cathode-side cooled F_m = 8... 12 kN			74	K/kW
Thermal resistance case to heatsink,	$R_{th(c-h)}$	Double-side cooled F_m = 8... 12 kN			7.5	K/kW
	$R_{th(c-h)}$	Single-side cooled F_m = 8... 12 kN			15	K/kW

Analytical function for transient thermal impedance:

$$Z_{th(j-c)}(t) = \sum_{i=1}^{n} R_i (1 - e^{-t/\tau_i})$$

i	1	2	3	4
R_i(K/kW)	19.18	9.820	5.450	1.440
τ_i(s)	0.3862	0.0561	0.0058	0.0024

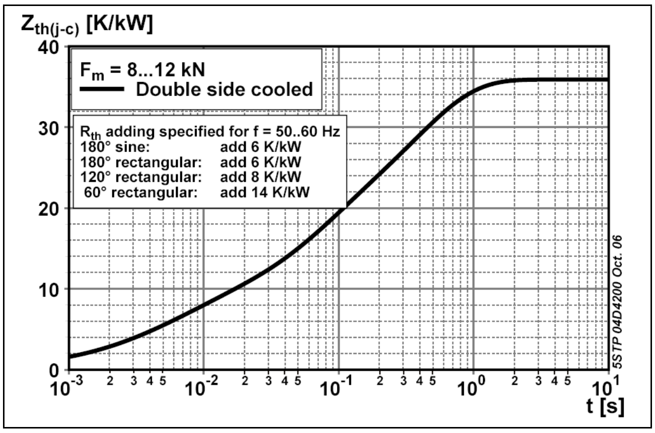


Fig. 1 Transient thermal impedance (junction-to-case) vs. time

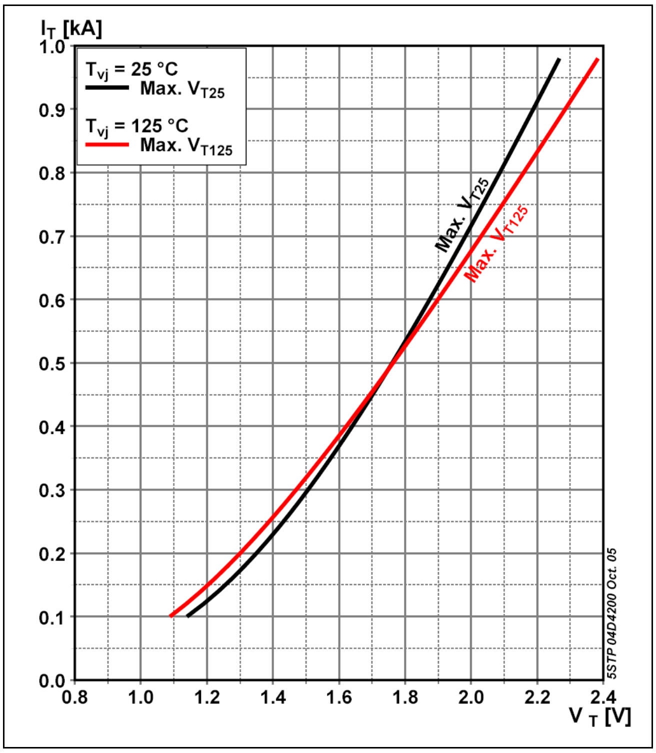


Fig. 2 On-state voltage characteristics

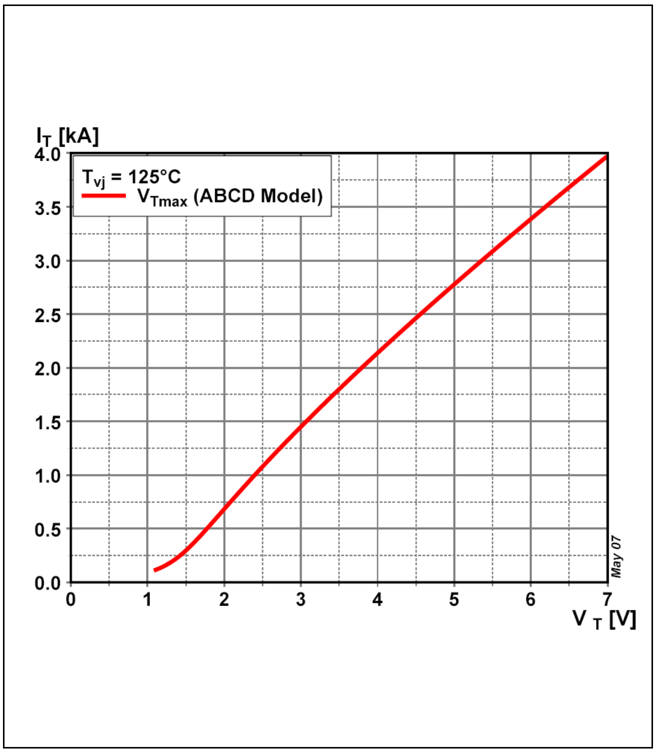


Fig. 3 On-state voltage characteristics
10 ms sine half wave

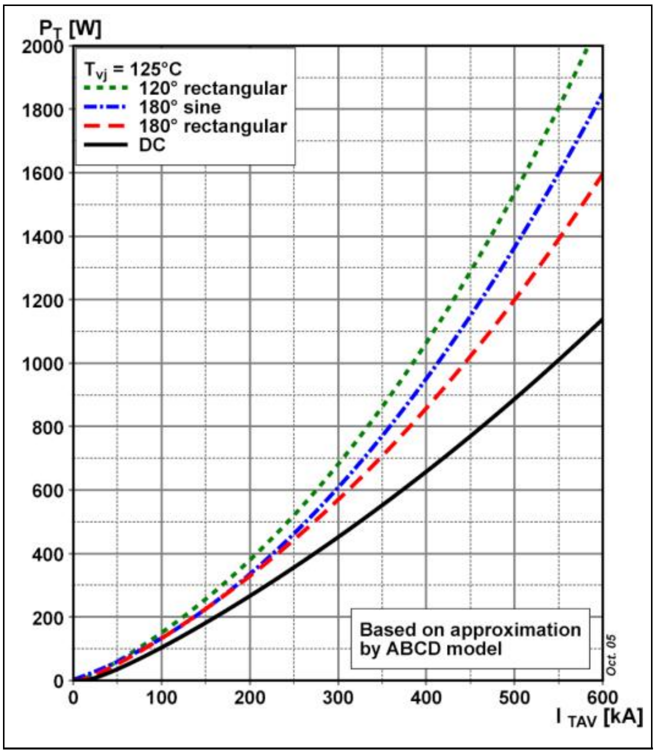


Fig. 4 On-state power dissipation vs. mean on-state current, turn-on losses excluded

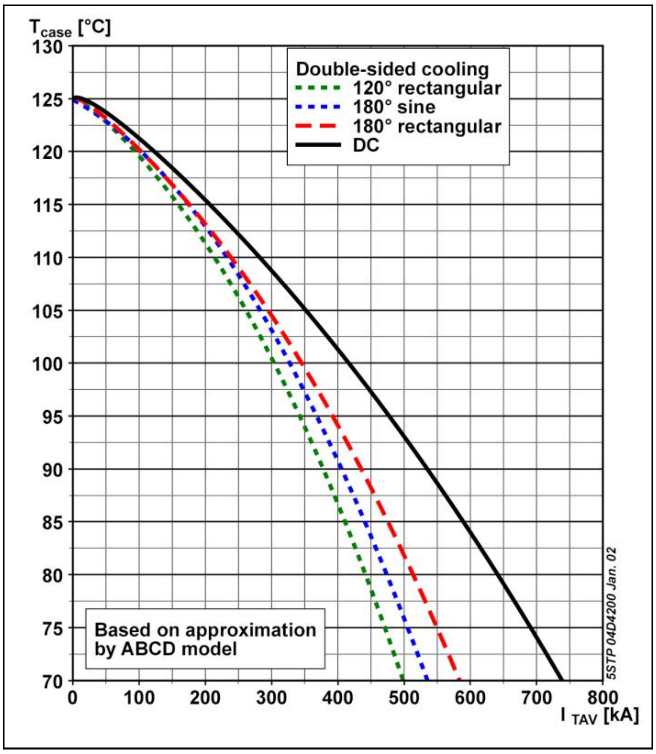


Fig. 5 Max. permissible case temperature vs. mean on-state current, switching losses ignored

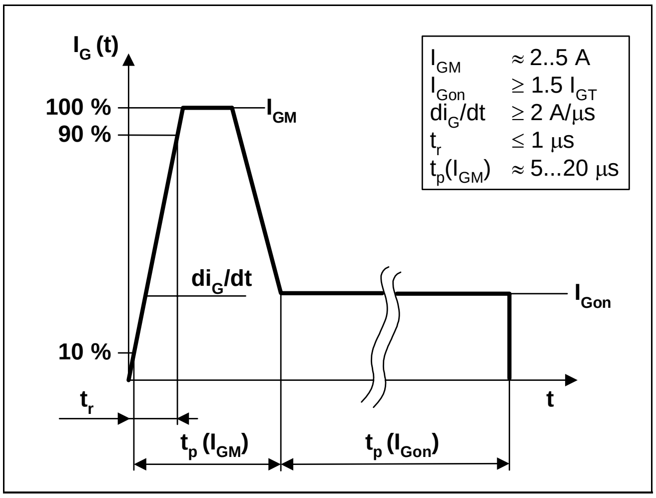


Fig. 6 Recommended gate current waveform

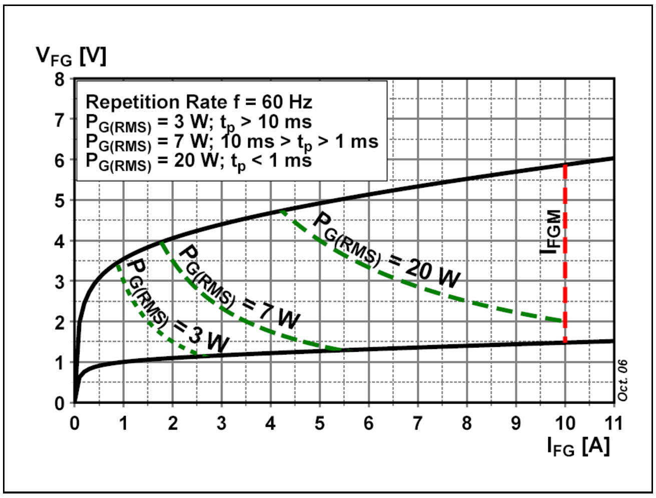


Fig. 7 Max. peak gate power loss

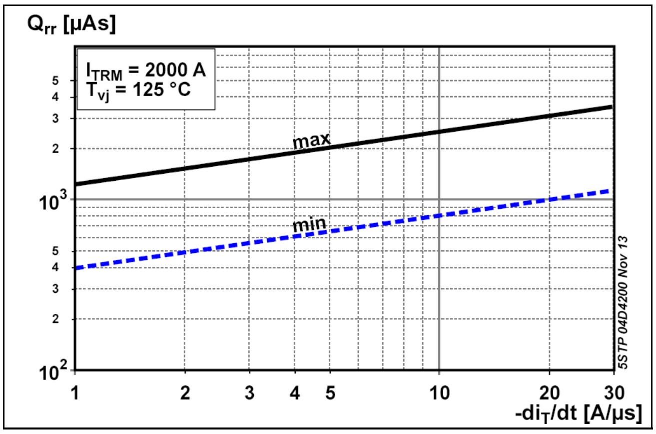


Fig. 8 Reverse recovery charge vs. decay rate of on-state current

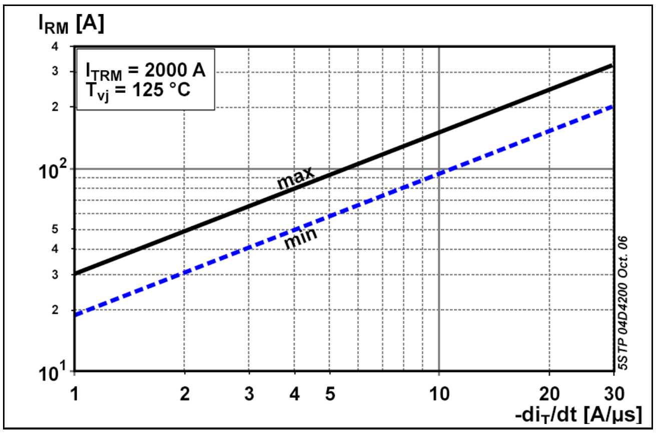


Fig. 9 Peak reverse recovery current vs. decay rate of on-state current

Turn-on and Turn-off losses

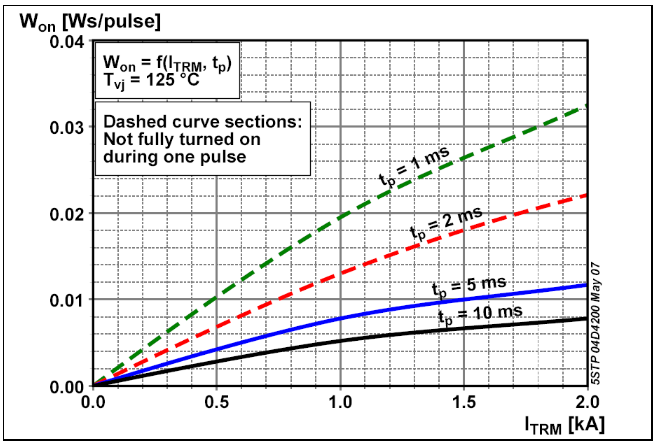


Fig. 10 Turn-on energy, half sinusoidal waves

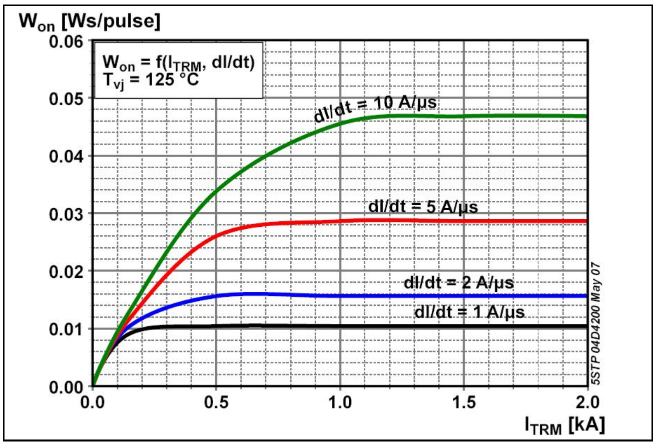


Fig. 11 Turn-on energy, rectangular waves

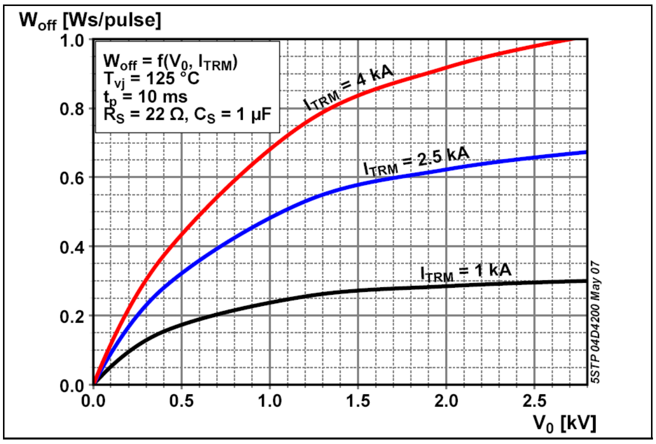


Fig. 12 Turn-off energy, half sinusoidal waves

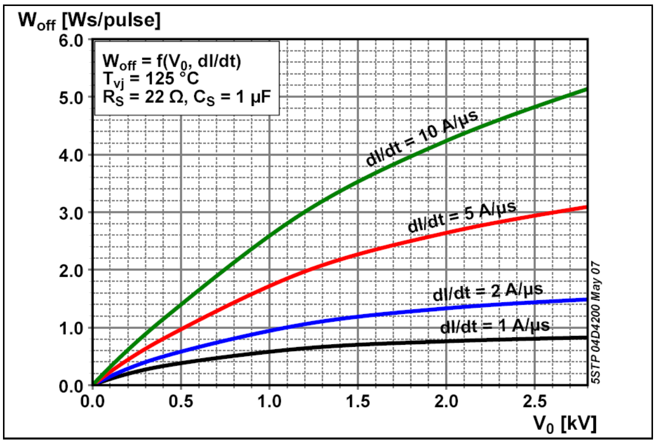


Fig. 13 Turn-off energy, rectangular waves

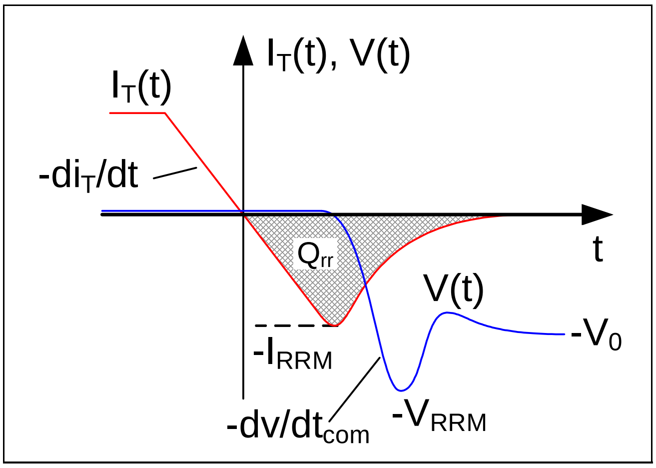


Fig. 14 Current and voltage waveforms at turn-off

Total power loss for repetitive waveforms:

$$P_{TOT} = P_T + W_{on} \cdot f + W_{off} \cdot f$$

where

$$P_T = \frac{1}{T}\int_0^T I_T \cdot V_T(I_T)\ dt$$

Fig. 15 Relationships for power loss

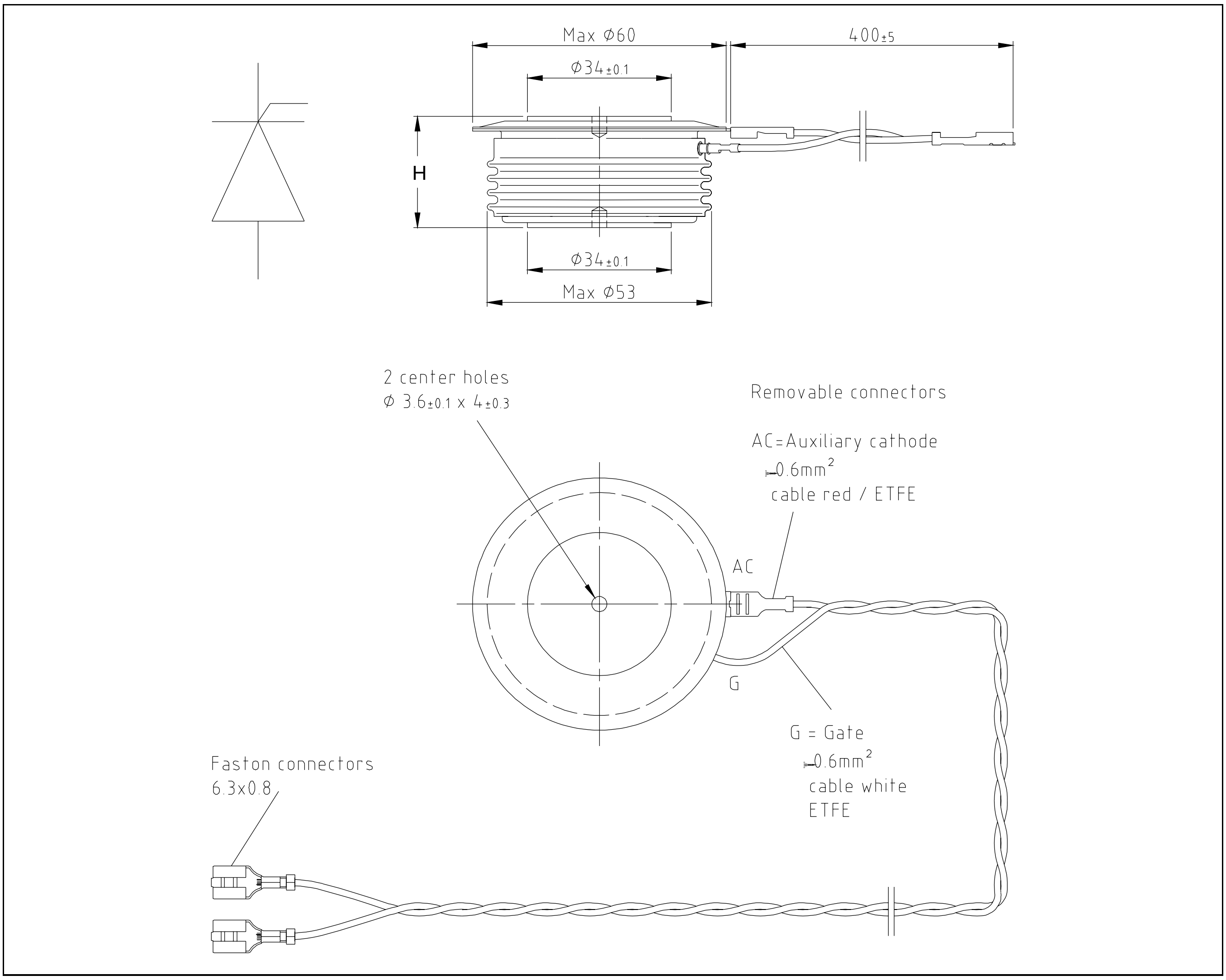


Fig. 16 Device Outline Drawing

Related documents:

5SYA 2020	Design of RC-Snubber for Phase Control Applications
5SYA 2049	Voltage definitions for phase control thyristors and diodes
5SYA 2051	Voltage ratings of high power semiconductors
5SYA 2034	Gate-Drive Recommendations for PCT's
5SYA 2036	Recommendations regarding mechanical clamping of Press Pack High Power Semiconductors
5SZK 9104	Specification of environmental class for pressure contact diodes, PCTs and GTO, STORAGE available on request, please contact factory
5SZK 9105	Specification of environmental class for pressure contact diodes, PCTs and GTO, TRANSPORTATION available on request, please contact factory

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