NXP PSMN1R1-30PL MOSFET datasheet

http://www.manuallib.com/nxp/psmn1r1-30pl-mosfet-datasheet.html

Logic level N-channel MOSFET in TO-220 package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

ManualLib.com collects and classifies the global product instrunction manuals to help users access anytime and anywhere, helping users make better use of products.

http://www.manuallib.com



N-channel 30 V 1.3 mΩ logic level MOSFET in TO-220 2 April 2014

Product data sheet

General description 1.

Logic level N-channel MOSFET in TO-220 package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

Features and benefits 2.

- High efficiency due to low switching and conduction losses •
- Suitable for logic level gate drive sources

Applications 3.

- DC-to-DC converters •
- Load switiching
- Motor control •
- Server power supplies •

Quick reference data 4.

Table 1. Qu	ick reference data						
Symbol	Parameter	Conditions		Min	Тур	Мах	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C		-	-	30	V
I _D	drain current	T _{mb} = 25 °C; V _{GS} = 10 V; <u>Fig. 2</u>	[1]	-	-	120	А
P _{tot}	total power dissipation	T _{mb} = 25 °C; <u>Fig. 1</u>		-	-	338	W
Tj	junction temperature			-55	-	175	°C
Static charac	teristics	·	I				
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; Fig. 12	[2]	-	1.1	1.3	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 100 °C; Fig. 13		-	1.5	1.8	mΩ
Dynamic cha	racteristics						-
Q _{GD}	gate-drain charge	V_{GS} = 4.5 V; I _D = 75 A; V _{DS} = 15 V;		-	37	-	nC
Q _{G(tot)}	total gate charge	<u>Fig. 14; Fig. 15</u>		-	118	-	nC





Scan or click this QR code to view the latest information for this product

PSMN1R1-30PL

N-channel 30 V 1.3 m Ω logic level MOSFET in TO-220

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
Avalanche ruggedness							
E _{DS(AL)S}	non-repetitive drain- source avalanche energy	$\label{eq:VGS} \begin{array}{l} V_{GS} = 10 \; V; \; T_{j(\text{init})} = 25 \; ^{\circ}\text{C}; \; I_{D} = 120 \; A; \\ V_{sup} \leq 30 \; V; \; R_{GS} = 50 \; \Omega; \; \text{unclamped} \end{array}$		-	-	1.9	J

[1] Continuous current is limited by package.

[2] Measured 3 mm from package.

5. Pinning information

Table 2.	Pinning	information		
Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	mb	D
2	D	drain		
3	S	source		G-UTA
mb	D	mounting base; connected to drain		mbb076 S
			TO-220AB (SOT78)	

6. Ordering information

Table 3. Ordering in	formation					
Type number	Package					
	Name	Description	Version			
PSMN1R1-30PL	TO-220AB	plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB	SOT78			

7. Marking

Table 4. Marking codes	
Type number	Marking code
PSMN1R1-30PL	PSMN1R1-30PL

PSMN1R1-30PL Product data sheet All information provided in this document is subject to legal disclaimers.
2 April 2014

Max

30

30

20

338

120

120

1609

175

175 260

120

1609

1.9

Unit

V

V

V

W

А

A

A

°C

°C

°C

А

А

J

N-channel 30 V 1.3 mΩ logic level MOSFET in TO-220

8. Limiting values

Table 5. **Limiting values** In accordance with the Absolute Maximum Rating System (IEC 60134). Conditions **Symbol Parameter** Min T_i ≥ 25 °C; T_i ≤ 175 °C V_{DS} drain-source voltage _ T_i ≥ 25 °C; T_i ≤ 175 °C; R_{GS} = 20 kΩ VDGR drain-gate voltage - V_{GS} gate-source voltage -20 T_{mb} = 25 °C; <u>Fig. 1</u> P_{tot} total power dissipation drain current V_{GS} = 10 V; T_{mb} = 100 °C; <u>Fig. 2</u> I_{D} [1] _ V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2 [1] pulsed; $t_p \le 10 \ \mu s$; $T_{mb} = 25 \ ^{\circ}C$; Fig. 3 peak drain current -I_{DM} -55 T_{stg} storage temperature Τj junction temperature -55 peak soldering temperature T_{sld(M)} _ Source-drain diode source current T_{mb} = 25 °C I_S [1] peak source current pulsed; $t_p \le 10 \ \mu s$; $T_{mb} = 25 \ ^{\circ}C$ I_{SM} -Avalanche ruggedness non-repetitive drain-source V_{GS} = 10 V; T_{i(init)} = 25 °C; I_D = 120 A; E_{DS(AL)S} _

[1] Continuous current is limited by package.

avalanche energy

PSMN1R1-30PL

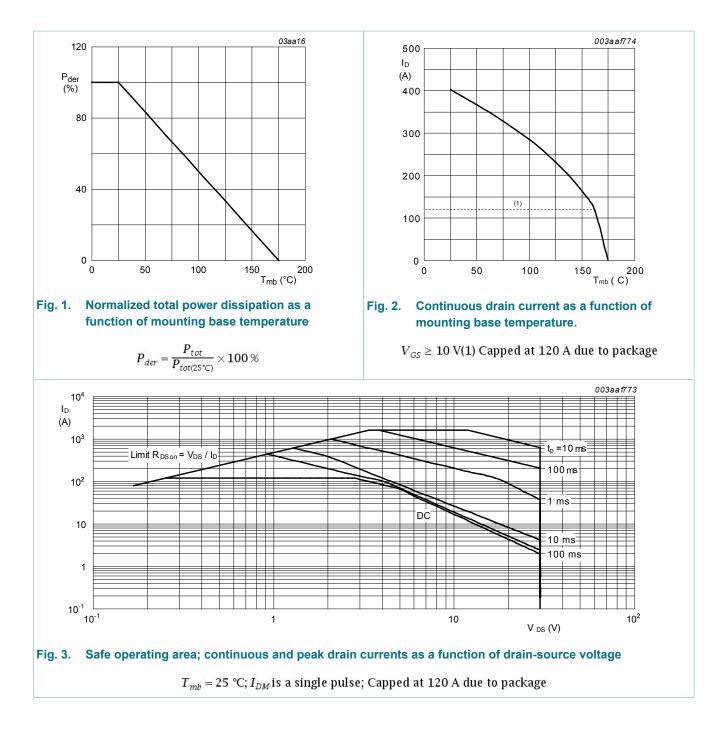
Product data sheet

All information provided in this document is subject to legal disclaimers.
2 April 2014

 $V_{sup} \le 30 \text{ V}; \text{ R}_{GS} = 50 \Omega; \text{ unclamped}$

PSMN1R1-30PL

N-channel 30 V 1.3 m Ω logic level MOSFET in TO-220



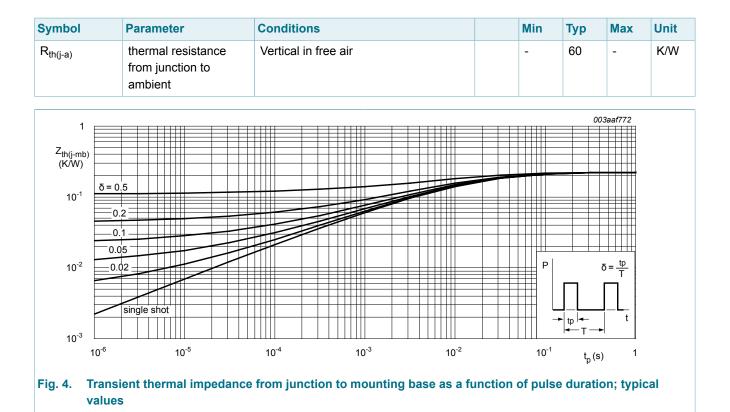
9. Thermal characteristics

Table 6. The	ermal characteristics					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R _{th(j-mb)}	thermal resistance from junction to mounting base	<u>Fig. 4</u>	-	0.22	0.44	K/W

PSMN1R1-30PL	All information provided in this document is subject to legal disclaimers.	© NXP Semiconductors N.V. 2014. All rights reserved
Product data sheet	2 April 2014	4 / 14

PSMN1R1-30PL

N-channel 30 V 1.3 m Ω logic level MOSFET in TO-220



10. Characteristics

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
Static chara	acteristics						
V _{(BR)DSS}	drain-source	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C		30	-	-	V
	breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C		27	-	-	V
	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS} ; T_j = 25 °C; Fig. 10; Fig. 11		1.3	1.7	2.2	V
		I _D = 2 mA; V _{DS} = V _{GS} ; T _j = 175 °C; Fig. 11		0.5	-	-	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = -55 °C; Fig. 11		-	-	2.5	V
I _{DSS}	drain leakage current	V _{DS} = 30 V; V _{GS} = 0 V; T _j = 25 °C		-	0.02	10	μA
		V _{DS} = 30 V; V _{GS} = 0 V; T _j = 175 °C		-	250	500	μA
I _{GSS}	gate leakage current	V_{GS} = 16 V; V_{DS} = 0 V; T_j = 25 °C		-	10	100	nA
		V _{GS} = -16 V; V _{DS} = 0 V; T _j = 25 °C		-	10	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; Fig. 12	[1]	-	1.1	1.3	mΩ

PSMN1R1-30PL Product data sheet All information provided in this document is subject to legal disclaimers.
2 April 2014

5/14

N-channel 30 V 1.3 m Ω logic level MOSFET in TO-220

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
		V _{GS} = 4.5 V; I _D = 25 A; T _j = 25 °C; <u>Fig. 12</u>	-	1.2	1.4	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 175 °C; Fig. 13; Fig. 12	-	2.1	2.5	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 100 °C; Fig. 13	-	1.5	1.8	mΩ
R _G	gate resistance	f = 1 MHz	-	1.1	-	Ω
Dynamic ch	naracteristics	· · · ·	I			
Q _{G(tot)} total gate charge		I _D = 75 A; V _{DS} = 15 V; V _{GS} = 10 V; Fig. 14; Fig. 15	-	243	-	nC
		I _D = 0 A; V _{DS} = 0 V; V _{GS} = 10 V; Fig. 14; Fig. 15	-	223	-	nC
		I_D = 75 A; V_{DS} = 15 V; V_{GS} = 4.5 V;	-	118	-	nC
Q _{GS}	gate-source charge	Fig. 14; Fig. 15	-	39	-	nC
Q _{GS(th)}	pre-threshold gate- source charge		-	22	-	nC
$Q_{GS(th-pl)}$	post-threshold gate- source charge		-	17	-	nC
Q _{GD}	gate-drain charge		-	37	-	nC
V _{GS(pl)}	gate-source plateau voltage	V _{DS} = 15 V; <u>Fig. 14; Fig. 15</u>	-	2.8	-	V
C _{iss}	input capacitance	V _{DS} = 15 V; V _{GS} = 0 V; f = 1 MHz;	-	14850	-	pF
C _{oss}	output capacitance	T _j = 25 °C; <u>Fig. 16</u>	-	2799	-	pF
C _{rss}	reverse transfer capacitance		-	1215	-	pF
t _{d(on)}	turn-on delay time	V_{DS} = 15 V; R _L = 0.2 Ω; V _{GS} = 4.5 V;	-	95	-	ns
t _r	rise time	$R_{G(ext)} = 5 \Omega; I_D = 75 A; T_j = 25 °C$	-	213	-	ns
t _{d(off)}	turn-off delay time		-	199	-	ns
t _f	fall time		-	115	-	ns
Source-drai	in diode		1			
V _{SD}	source-drain voltage	I_{S} = 25 A; V_{GS} = 0 V; T_{j} = 25 °C; <u>Fig. 17</u>	-	0.8	1.2	V
t _{rr}	reverse recovery time	$I_{\rm S}$ = 25 A; dI_{\rm S}/dt = -100 A/µs; V _{GS} = 0 V;	-	67	-	ns
Q _r	recovered charge	V _{DS} = 15 V	-	123	-	nC

[1] Measured 3 mm from package.

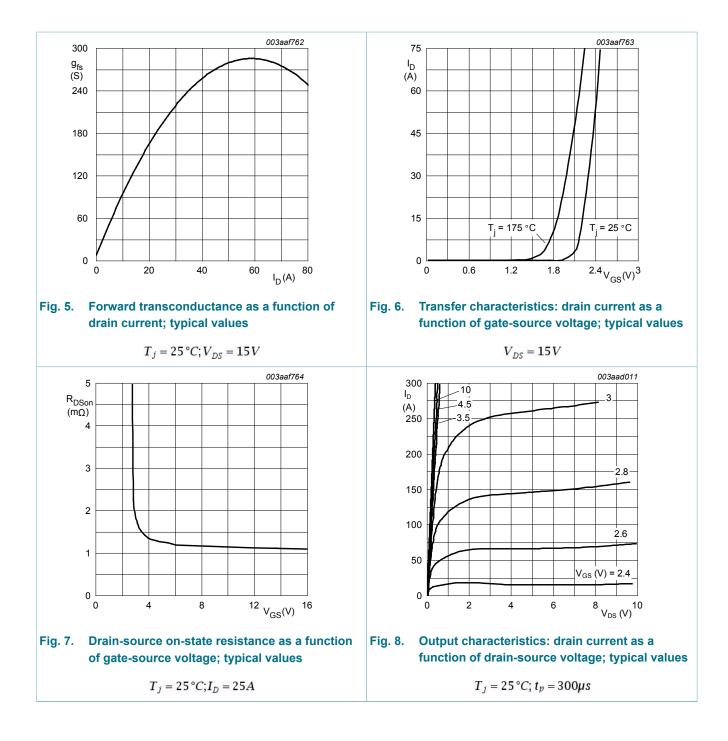
PSMN1R1-30PL

Product data sheet

All information provided in this document is subject to legal disclaimers.

PSMN1R1-30PL

N-channel 30 V 1.3 m Ω logic level MOSFET in TO-220

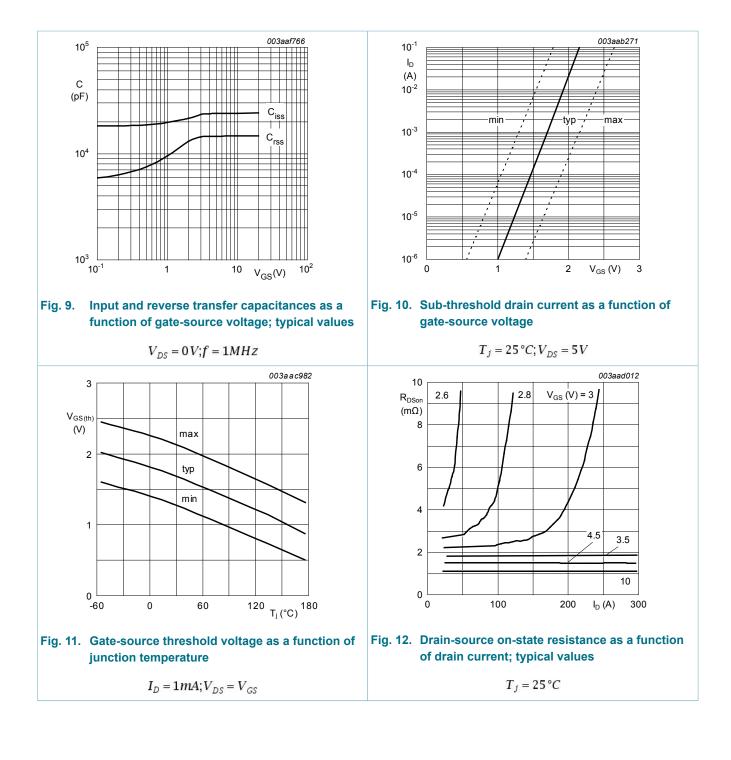


PSMN1R1-30PL Product data sheet All information provided in this document is subject to legal disclaimers.
2 April 2014

7/14

PSMN1R1-30PL

N-channel 30 V 1.3 m Ω logic level MOSFET in TO-220

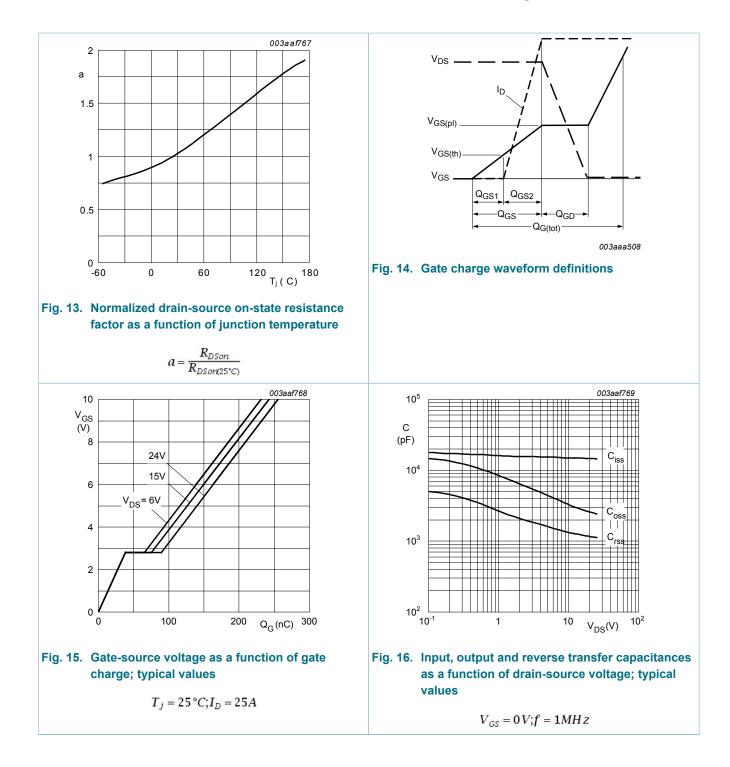


PSMN1R1-30PL Product data sheet All information provided in this document is subject to legal disclaimers.

8/14

PSMN1R1-30PL

N-channel 30 V 1.3 mΩ logic level MOSFET in TO-220

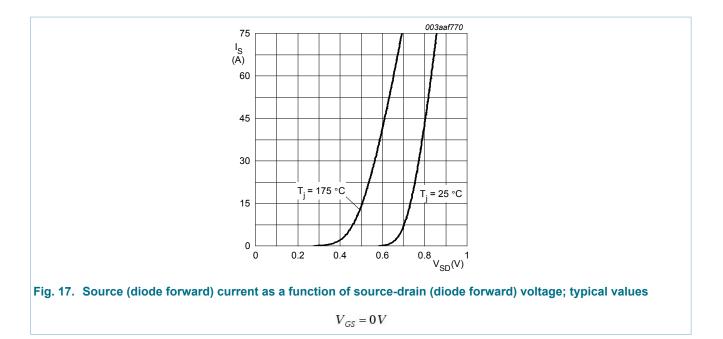


PSMN1R1-30PL Product data sheet All information provided in this document is subject to legal disclaimers.
2 April 2014

9/14

PSMN1R1-30PL

N-channel 30 V 1.3 m Ω logic level MOSFET in TO-220



PSMN1R1-30PL

2 April 2014

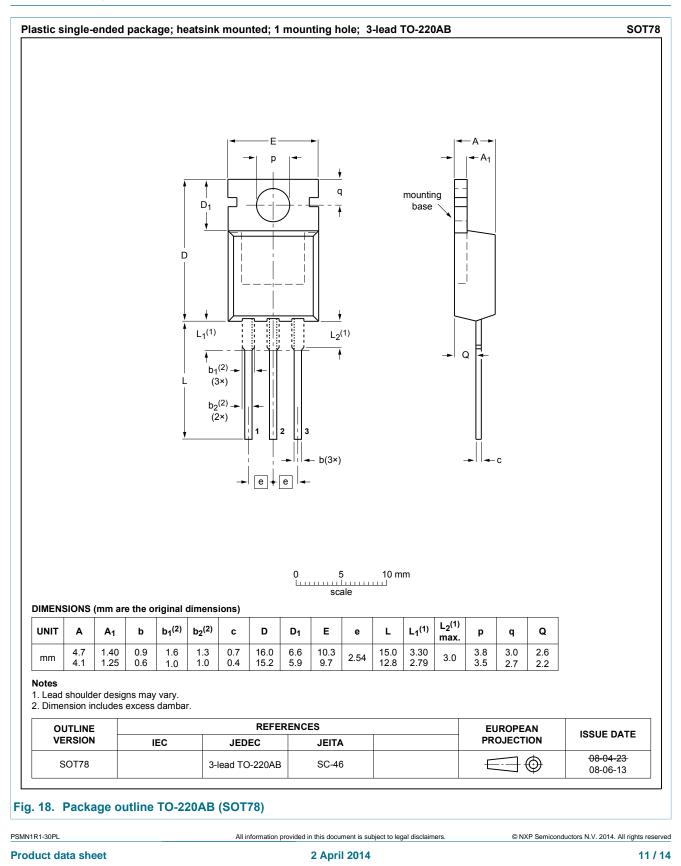
All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved 10 / 14

Product data sheet

N-channel 30 V 1.3 mΩ logic level MOSFET in TO-220

11. Package outline



N-channel 30 V 1.3 mΩ logic level MOSFET in TO-220

12. Legal information

12.1 Data sheet status

Document status [1][2]	Product status [<u>3]</u>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

 The term 'short data sheet' is explained in section "Definitions".
 The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <u>http://www.nxp.com</u>.

12.2 Definitions

Preview — The document is a preview version only. The document is still subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

12.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the

PSMN1R1-30PL

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved

Product data sheet

2 April 2014

12/14

N-channel 30 V 1.3 mΩ logic level MOSFET in TO-220

grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

12.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

Adelante, Bitport, Bitsound, CoolFlux, CoReUse, DESFire, EZ-HV, FabKey, GreenChip, HiPerSmart, HITAG, I²C-bus logo, ICODE, I-CODE, ITEC, Labelution, MIFARE, MIFARE Plus, MIFARE Ultralight, MoReUse, QLPAK, Silicon Tuner, SiliconMAX, SmartXA, STARplug, TOPFET, TrenchMOS, TriMedia and UCODE — are trademarks of NXP Semiconductors N.V.

HD Radio and HD Radio logo — are trademarks of iBiquity Digital Corporation.

Product data sheet

PSMN1R1-30PL

All information provided in this document is subject to legal disclaimers.
2 April 2014

N-channel 30 V 1.3 mΩ logic level MOSFET in TO-220

13. Contents

1	General description	1
2	Features and benefits	1
3	Applications	1
4	Quick reference data	1
5	Pinning information	2
6	Ordering information	2
7	Marking	2
8	Limiting values	3
9	Thermal characteristics	4
10	Characteristics	5
11	Package outline	11
12	Legal information	12
12.1	Data sheet status	12
12.2	Definitions	12
12.3	Disclaimers	12
12.4	Trademarks	

© NXP Semiconductors N.V. 2014. All rights reserved

For more information, please visit: http://www.nxp.com For sales office addresses, please send an email to: salesaddresses@nxp.com Date of release: 2 April 2014

PSMN1R1-30PL Product data sheet All information provided in this document is subject to legal disclaimers. 2 April 2014

© NXP Semiconductors N.V. 2014. All rights reserved

14/14