

# **NXP AN11508 Electronic components Application note**

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This document describes some of the issues that you may encounter when developing a full-speed USB application on NXP's LPC microcontrollers. Possible solutions are detailed.

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# AN11508

## SDRAM interface to LPC18xx/43xx EMC

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Application note

### Document information

Info	Content
<b>Keywords</b>	LPC1800, LPC18xx, LPC4300, LPC43xx, SDRAM, EMC
<b>Abstract</b>	This application note describes how to properly interface SDRAM memory to the LPC1800 and LPC4300 External Memory Controller.



**Revision history**

Rev	Date	Description
1	20140124	Initial release.

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## 1. Introduction

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The LPC18xx and LPC43xx 32-bit microcontroller families were designed for embedded applications requiring high performance and low power consumption. The LPC43xx is a dual-core microcontroller implementing an ARM Cortex-M4 and an ARM Cortex-M0 core. The ARM Cortex-M4 is used as application processor. The second core, the ARM Cortex-M0, can be used as co-processor to off-load the ARM Cortex-M4 and to perform serial I/O tasks. The LPC18xx is a single core microcontroller implementing an ARM Cortex-M3 core. The LPC18xx/43xx include an on-chip SRAM, a quad SPI Flash Interface (SPIFI), advanced configurable peripherals such as the State Configurable Timer (SCT), two High-speed USB controllers, Ethernet, LCD, an external memory controller, and multiple digital and analog peripherals. The LPC43xx operate at CPU frequencies of up to 204 MHz, while the LPC18xx operate at CPU frequencies of up to 180 MHz.

The LPC43xx and LPC18xx use the same External Memory Controller (EMC), an ARM PrimeCell MultiPort Memory Controller peripheral offering support for asynchronous static memory devices such as RAM, ROM and Flash, as well as dynamic memories such as Single Data Rate (SDR) SDRAM. For microcontroller external memory of 2 MB or larger the SDR SDRAM is one of the most practical memories to use today.

This application note will focus on interface connectivity and board layout guidelines when using SDR SDRAM memories with the LPC18xx/43xx microcontrollers.

The LPC18xx or LPC43xx user manuals will be referenced in this application note, so keep the corresponding user manual (LPC18xx UM10430; LPC43xx UM10530) at hand.

## 2. External Memory Controller (EMC)

The LPC18/43xx EMC is an ARM PrimeCell MultiPort Memory Controller peripheral offering support for asynchronous static memory devices such as RAM, ROM and Flash, as well as dynamic memories such as SDR SDRAM. The EMC does not support double data rate (DDR) SDRAMs, or synchronous static memory devices (synchronous burst mode).

### 2.1 EMC signals

The EMC supports up to a 32-bit data bus, depending on which device package is used. The EMC supports a 16-bit or 32-bit wide data interface built from 8, 16 or 32-bit SDRAM chips. The static memory data bus may be 8-bit, 16-bit or 32-bit when mixed with SDRAM. The EMC signals are multiplexed at the chip port pins with other functions. Some EMC functions are available only at a single port pin while others are available at multiple port pins. The selection of which port pin to use may depend on what other chip peripherals will be used. Use the appropriate data sheet to select the required EMC functions for SRAM and SDRAM support. The EMC functions required for interfacing with SDRAM and SRAM are listed in [Table 1](#).

**Table 1. EMC signals**

EMC signal	Static RAM function	SDRAM function	Notes
EMC_A12:0	Memory address	Row / column address	A0, A9:6 also used for boot mode select.
EMC_A14:13	Memory address	Bank	EMC_A13 to Bank0; EMC_A4 to Bank1.
EMC_A23:15	Memory address	-	Not used with SDRAM.
EMC_D31:0	Data	Data	SRAM 8-bit, 16-bit, 32-bit; SDRAM 16-bit, 32-bit.
EMC_OE	Output enable strobe	-	Active low, not used with SDRAM
EMC_BLS3:0	Byte lane select / byte write enable		Active low. Specific behavior is controlled by STATICCONFIG[0:3] register PB bit.
EMC_CS3:0	Chip select		Active low, not used with SDRAM
EMC_WE	Write enable	Write enable	Active low. Defines command to SDRAM. SRAM Specific behavior is controlled by STATICCONFIG[0:3] register PB bit.
EMC_DYCS3:0	-	Chip select	Active low. Reference the user manual for AHB address range for each select space. Not used with SRAM.
EMC_CKEOUT3:0	-	Clock enable	Active low, one for each DYCS. Not used with SRAM.
EMC_CAS	-	Column address strobe	Defines command to SDRAM along with RAS, WE and DYCS. Not used with SRAM.

EMC signal	Static RAM function	SDRAM function	Notes
EMC_RAS	-	Row address strobe	Defines command to SDRAM along with CAS, WE and DYCS. Not used with SRAM.
EMC_DQMOUT3:0	-	Data mask	Active high, one mask bit for each data byte lane.
EMC_CLK3:0	-	Clock	One clock for each data byte lane. Use when 8-bit wide SDRAMs form 16 or 32-bit system memory. When x32 data width SDRAM is used, EMC_CLK1 or EMC_CLK3 may be used to drive SDRAM clock while EMC_CLK01 and EMC_CLK23 are used for FBCLK. Not used with SRAM.
EMC_CLK01	-	Clock	Combined clock available on CLK0 pin. Not used for SRAM
EMC_CLK23	-	Clock	Combined clock available on CLK2 pin. Not used for SRAM.

## 2.2 EMC clocking to SDRAM

There are two clock options for the EMC\_CCLK. For the LPC18xx either BASE\_M3\_CLK or 1/2 x BASE\_M3\_CLK core clock may be used. For the LPC43xx the BASE\_M4\_CLK or 1/2 x BASE\_M4\_CLK core clock may be used. If the EMC\_CCLK is configured for 1/2 x BASE\_M3\_CLK or 1/2 x BASE\_M4\_CLK, the CLK\_M3\_EMCDIV or CLK\_M4\_EMCDIV branch clock must be configured for half-frequency clock operation in both the CREG6 register and the CCU1 CLK\_EMCDIV\_CFG register.

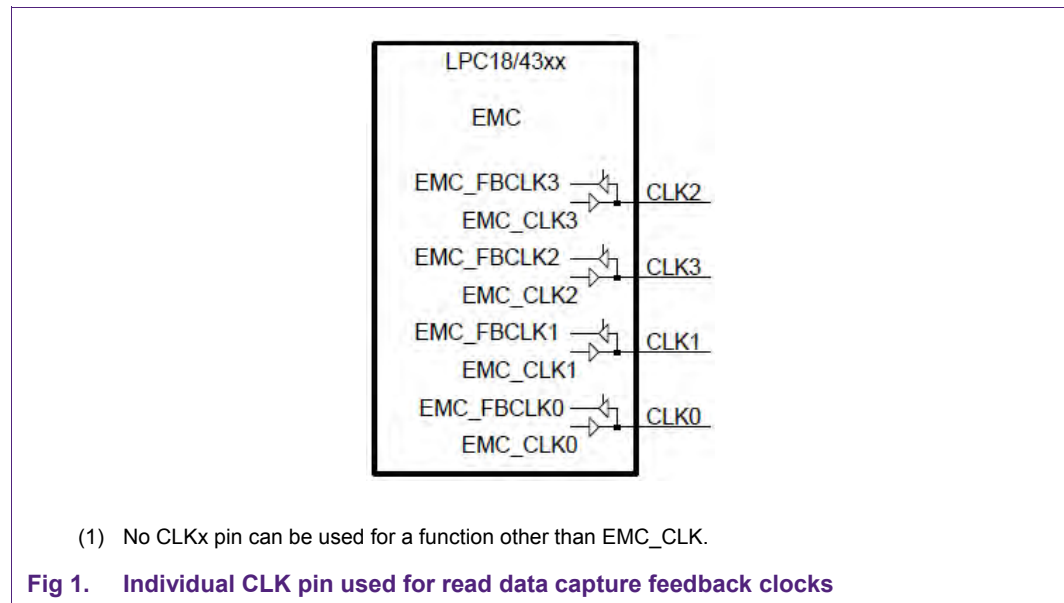
At the SDRAM, all input signals are sampled on the positive edge of the clock pin. The clock pin also increments the SDRAM internal burst counter and controls the output registers.

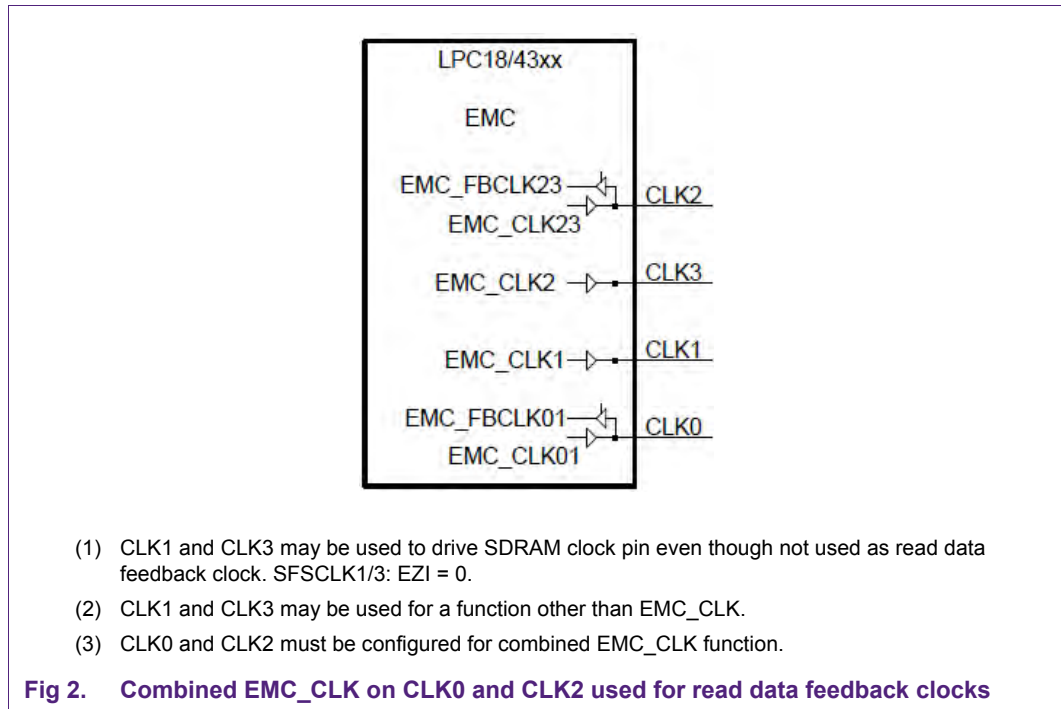
### 2.2.1 EMC\_CLK3:0 signal pin configuration

The EMC dynamic memory interface has four clocks (EMC\_CLK3:0), one for each EMC data byte lane. The EMC may be configured for either a 16-bit wide or 32-bit wide SDRAM system memory. The EMC\_CLK3:0 signals are output on pins CLK3:0. It is essential that all four EMC\_CLK3:0 signals get fed back to the EMC block for the SDRAM interface to read data from the SDRAM correctly. To use SDRAM, regardless of the EMC data width, you must have all four byte lane feedback clocks configured in the System Control Unit (SCU). You may use all four CLKx pins, one for each EMC\_CLKx signal, by setting SFSCCLKx mode to function 0 (see [Fig 1](#)). Alternatively, SFSCCLK0 may be configured for combined EMC\_CLK01 (function 5), and SFSCCLK2 may be configured for combined EMC\_CLK23 (function 5), as shown in [Fig 2](#). When CLK0 and CLK2 pins are configured for function 5, CLK1 and CLK3 pins may be used to drive the SDRAM clock pin, or used for a function other than the EMC\_CLK. The mapping between the CLKx pin and EMC\_CLKx signal and typical settings for SFSCCLKx register are shown in [Table 2](#). The common CLKx pin combinations used for SDRAM configurations are shown in [Fig 3](#).

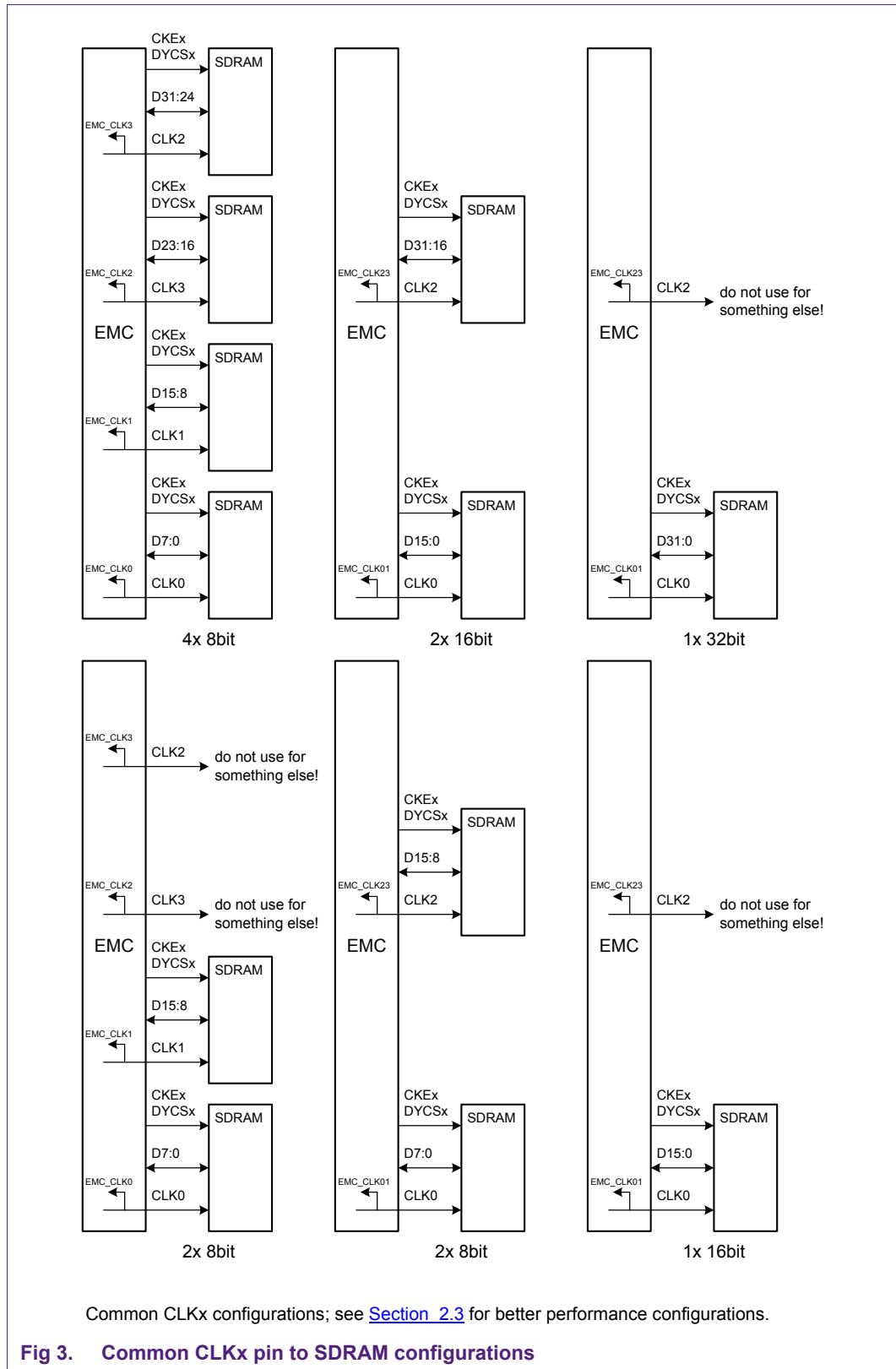
**Table 2. CLKx pin configuration**

Pin name	EMC_CLK	SFSCCLK:Mode	ZIF, EZI, EHS, EPUN, EPD
CLK0	EMC_CLK0	Function 0	1, 1, 0, 1, 0
CLK0	EMC_CLK01	Function 5	1, 1, 0, 1, 0
CLK1	EMC_CLK1	Function 0	1, 1, 0, 1, 0
CLK2	EMC_CLK3	Function 0	1, 1, 0, 1, 0
CLK2	EMC_CLK23	Function 5	1, 1, 0, 1, 0
CLK3	EMC_CLK2	Function 0	1, 1, 0, 1, 0









2.2.2 EMC output signal timing to SDRAM

At the SDRAM, all input signals are sampled on the positive edge of the clock pin. The Dynamic memory read configuration register DYNAMICREADCONFIG:RD together with the EMC clock delay register (EMCDELAYCLK) are used to ensure proper setup and hold times for EMC signals registered by the SDRAM. With the Dynamic Memory Read Configuration register DYNAMICREADCONFIG:RD = 0x1, all EMC signals, except the CLKx and CKEx, are delayed by 1/2 EMCCCLK period. This means the EMC output signals change within a few nanoseconds after the falling edge of the internal EMCCLK, providing setup for the SDRAM to latch the command or data on the next rising edge of external EMC CLKx, as shown in Fig 4. The EMC clock delay register EMCDELAYCLK (0x40086D00) provides a programmable delay for the EMC\_CLKx outputs. Generally, the delay for all EMC\_CLKx outputs should be set the same, even if they aren't all going to an SDRAM. The CLKDLYx increases approximately 0.5 ns for each step from 0 (CLK\_DELAY = 0) to 3.5 ns (CLK\_DELAY = 0x00007777). The exact values of the delays vary over temperature and processing. It is recommended that EMCDELAYCLK be set to the lowest value necessary to meet the SDRAM minimum setup timing.

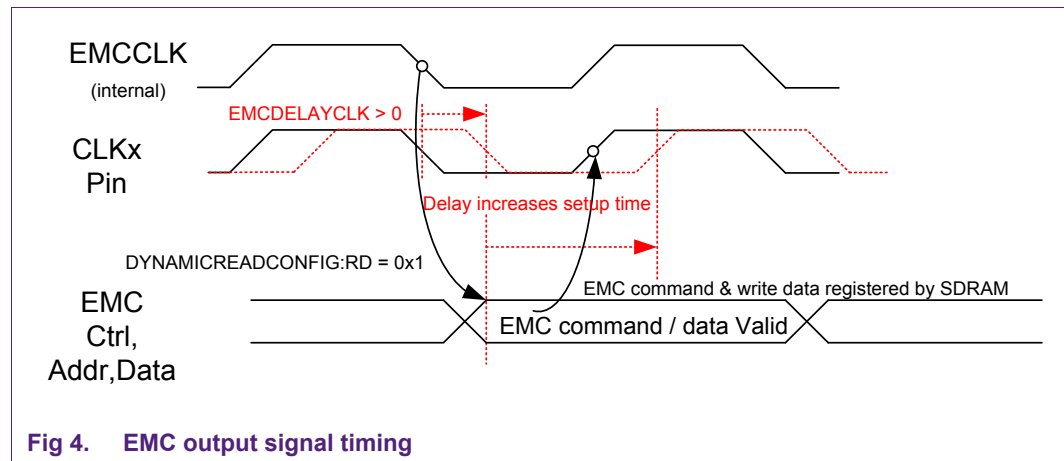


Fig 4. EMC output signal timing

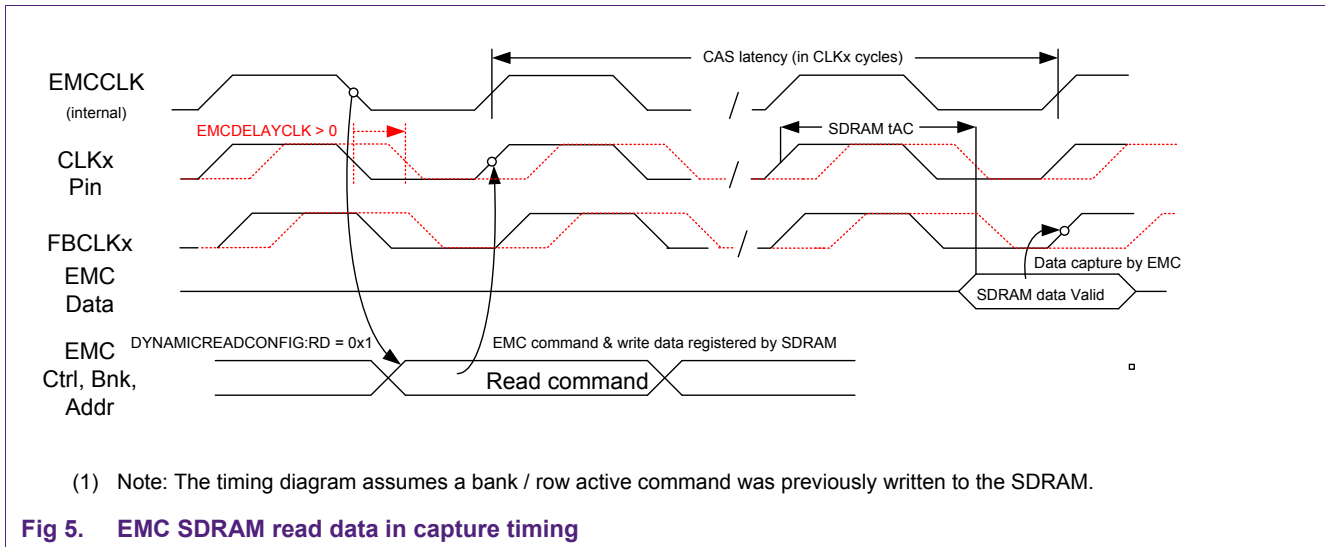
2.2.3 EMC signal capture read data timing from SDRAM

The EMC supports a 32-bit or 16-bit wide data interface built from x8, x16 or x32-bit SDRAM devices. The external data width and organization will determine which feedback clocks (FBCLKx) the EMC uses to pack the data in 32b words (see Table 3). Note that even when a single CLKx pin is used to drive a single SDRAM clock, at minimum CLK0 and CLK2 pins are used to feedback byte lane clocks for capturing read data from the SDRAM. The input buffer enable (EZI) must be set in the SFCLKx pin configuration register for the pin to source a feedback clock. The timing from the EMC issuing the read command to the SDRAM to the first word of a read burst from the SDRAM captured at the EMC is shown in Fig 5. The CAS latency is generally three SDRAM clock cycles. The same number of CAS latency clock cycles must match between the EMC Dynamic Memory RASCAS Delay registers DYNAMICRASCASx: CAS and the SDRAM Mode register CAS field. See the LPC18xx/43xx user's manual for a detailed example of what value to set the SDRAM mode register, and how to calculate the mode register address.

**Table 3. Read Data feedback clock mapping**

External SDRAM	DIN[31:24]	DIN[23:16]	DIN[15:8]	DIN[7:0]
32b (4x8b)[1]	EMC_CLK3	EMC_CLK2	EMC_CLK1	EMC_CLK0
32b (2x16b)[2]	EMC_CLK23	EMC_CLK23	EMC_CLK01	EMC_CLK01
32b (1x32b)[2][4]	EMC_CLK23[3]	EMC_CLK23[3]	EMC_CLK01	EMC_CLK01
16b (2x8b)[1]	EMC_CLK3[3]	EMC_CLK2	EMC_CLK1[3]	EMC_CLK0
16b (2x8b)[2]	EMC_CLK23	EMC_CLK23	EMC_CLK01	EMC_CLK01
16b (1x16)[2][4]	EMC_CLK23[3]	EMC_CLK23[3]	EMC_CLK01	EMC_CLK01

- [1] Use SFSCCLK pin configuration mode function 0 for CLK0, CLK1, CLK2, CLK3.
- [2] Use SFSCCLK pin configuration mode function 5 for CLK0, CLK2. Pins CLK1 and CLK3 may be used for alternate function.
- [3] These CLKx pins must have EZI = 1 in the SFSCCLKx register, but are not connected to SDRAM.
- [4] When using EMC\_CLK\_DIV2 mode with a single x16 or x32 SDRAM device, connecting CLK1 or CLK3 to the SDRAM may allow higher EMC clock speed. See section 2.2.5.2 for additional details.



**Fig 5. EMC SDRAM read data in capture timing**

### 2.2.4 Compensating for signal flight time delay

The time delay between the EMCCLK launched from the LPC43xx/18xx pin and a valid clock signal voltage arrival at the SDRAM is called flight time. Similarly, there is flight time between data being launched from the SDRAM and the signal reaching valid voltage level at the EMC. A 50 ohm PCB trace has approximately 1 ns of delay for every 6" of length. The data set-up time for read data captured at the EMC is reduced by the flight time of the EMCCLK to the SDRAM and the read data flight time from the SDRAM to EMC. With the EMC\_CLK at 102 MHz there is usually enough margin in the data setup time at the EMC for this flight time to be ignored. However, if the SDRAM is placed such that the flight time delay causes the read data to no longer arrive at the EMC early enough to meet the LPC43xx/18xx data input set-up time, either the EMCCLK speed needs to be reduced, or the EMC feedback clock delay register can be used to compensate for the flight time.

#### 2.2.4.1 EMC feedback clock delay register

This register provides a programmable delay for the EMC feedback clocks (8 data lanes per feedback clock). The delay for each control output is approximately 0.5 ns x XXX\_DELAY. (XXX\_DELAY = 0x0 ≈ 0 ns, 0x1: delay ≈ 0.5 ns, ... 0x7: delay ≈ 3.5 ns.)

The feedback clock delay register EMCFBCLKDELAY is found at address 0x40086d10. FBCLK0\_DELAY defined in bits 2:0, FBCLK1\_DELAY defined in bits 6:4, FBCLK2\_DELAY defined in bits 10:8, FBCLK3\_DELAY defined in bits 14:12. At reset all feedback delay bits are 0. All FBCLKx\_DELAYS are generally set to the same value.

### 2.2.5 Core clock divide by 2

When  $1/2 \times \text{BASE\_M4\_CLK}$  core clock (EMC\_CLK\_DIV) is used (also applies to  $1/2 \times \text{BASE\_M3\_CLK}$ ), the EMC\_CLKx duty cycle may become unsymmetrical where the high period is stretched longer and the low period becomes shorter. Since the EMC signals are launched from EMC on the falling edge of the EMC\_CLK, the impact of the shorter low period is the EMC signals will have less setup time before the next rising edge of EMC\_CLKx where they are registered by the SDRAM. When using EMC\_CLK\_DIV2 the EMCDELAYCLK value may need to be increased to obtain the same setup time provided when using the BASE\_M4\_CLK. For chip revisions that have an unsymmetrical EMC\_CLKx duty cycle when operating in  $1/2 \times \text{BASE\_Mx\_CLK}$  core clock mode, setting the EMCDELAYCLK value for all CLKx between 4 and 6 works best. Refer to chip errata sheet ES\_LPC43x0 or ES\_LPC18x0 section EMC.1 to determine if the chip revision you're using will have an unsymmetrical EMC\_CLKx duty cycle.

#### 2.2.5.1 Maximum EMC\_CLKx speed vs trace length

When using a CLKx pin to drive the SDRAM clock, and also as the feedback clock for capturing SDRAM read data, the maximum EMC speed will be determined by the round trip delay of the CLKx signal. This would apply to any of the common EMC clock configurations shown in [Fig 3](#). This is due to the way the source impedance of the high speed / high slew rate buffer driver and the PCB trace characteristic impedance together create a voltage divider at the pad of the CLKx signal, where the full signal swing at the CLKx pin receiver only occurs after the clock signal has propagated to the end of the PCB trace and has reflected back to the receiver.<sup>1 2</sup> As a worst case example, when using the core clock divide by 2 mode with a chip revision having an unsymmetrical EMC\_CLKx duty cycle and 6" of PCB trace length (having approximately 2 nS round-trip delay), the maximum functional EMC clock speed will be approximately 100 MHz (core speed 200 MHz).

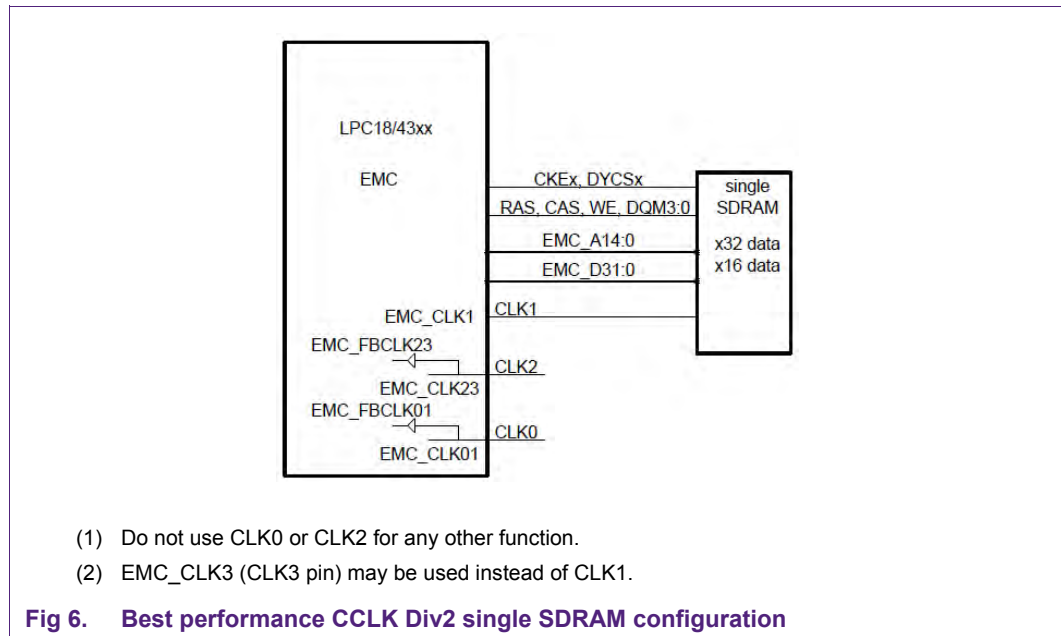
#### 2.2.5.2 Solution to achieve full system core / EMC clock speed (204 / 102 MHz)

The key to running the EMC at full speed is to use EMC\_CLK01 (CLK0 pin with SFSCCLK0 = function 5) and EMC\_CLK23 (CLK2 pin with SFSCCLK2 = function 5) for the four byte lane feedback clocks, while using EMC\_CLK1 (CLK1 pin) and / or EMC\_CLK2 (CLK3 pin) to drive the SDRAM clocks. LPC18/43xx pins CLK0/2 remain floating or connected to short PCB traces for access test points and therefore have immediate full swing signal at the feedback clock receiver input. Since CLK1 and CLK3 are not being used as feedback clocks their length may exceed the 6" restriction without affecting the feedback clocks for capturing SDRAM read data. For an example of using this solution with a single x16 or x32 SDRAM see [Fig 6](#) and [Fig 7](#). For an example using two x16 SDRAMs see [Fig 8](#).

1. For a better understanding of this behavior see "Right the First Time, A practical handbook on high speed PCB and system design", Volume one, chap 17, Lee Ritchey, 2003.
2. See NXP Application note AN246 Transmission lines and terminations with Philips Advanced Logic families, Source termination methods section.  
[http://www.nxp.com/documents/application\\_note/AN246.pdf](http://www.nxp.com/documents/application_note/AN246.pdf)

### 2.2.5.3 Best performance using a single SDRAM device and CCLK Div2

When using a single SDRAM, x16 or x32, a single CLKx pin is connected between the EMC and the SDRAM as shown in Fig 6. However, all four EMC feedback clocks (EMC\_FBCLKx) are needed for capturing read data from the SDRAM (see section 2.2.3 for details). See section 2.6 for recommended termination near the SDRAM.



## 2.3 EMC to SDR SDRAM connections

The LPC32x0 EMC supports either a 16-bit wide or 32-bit wide system SDR SDRAM bus. The system SDR SDRAM bus may be constructed with:

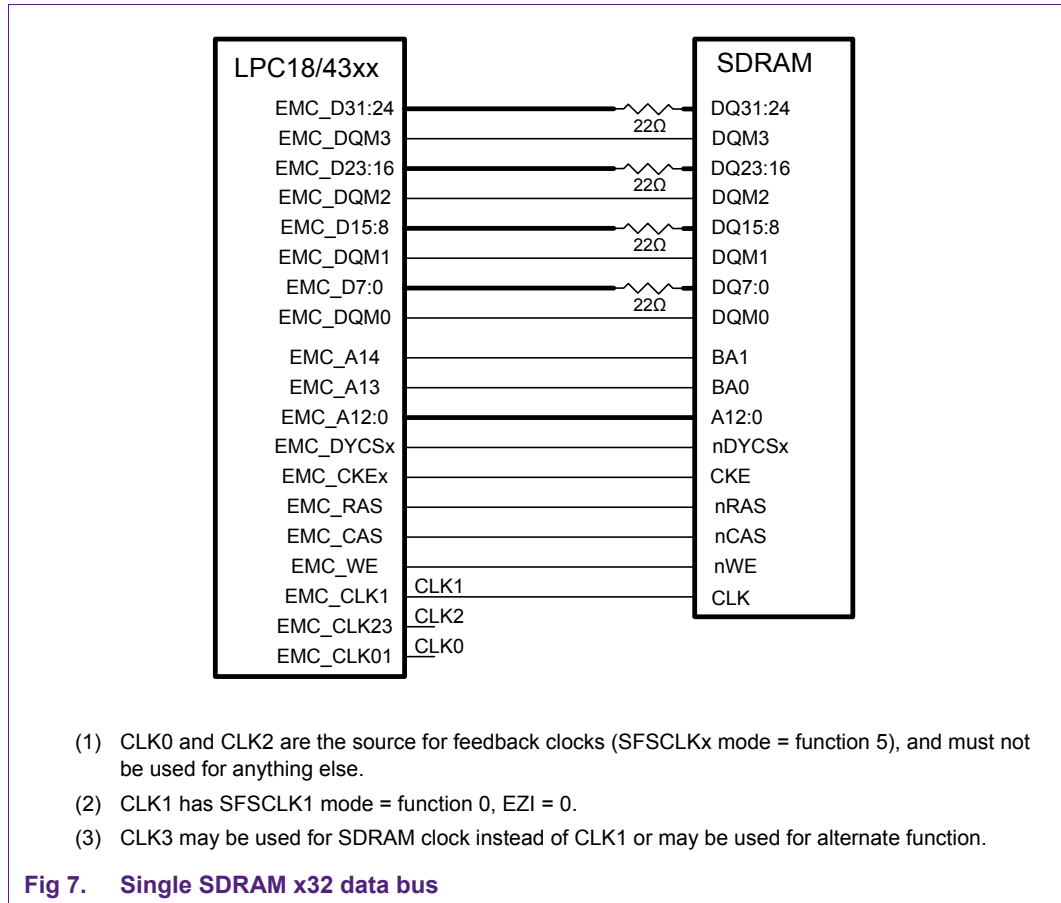
- one 32-bit wide SDR SDRAM
- one or two 16-bit wide SDR SDRAMs
- two or four 8-bit wide SDR SDRAMs

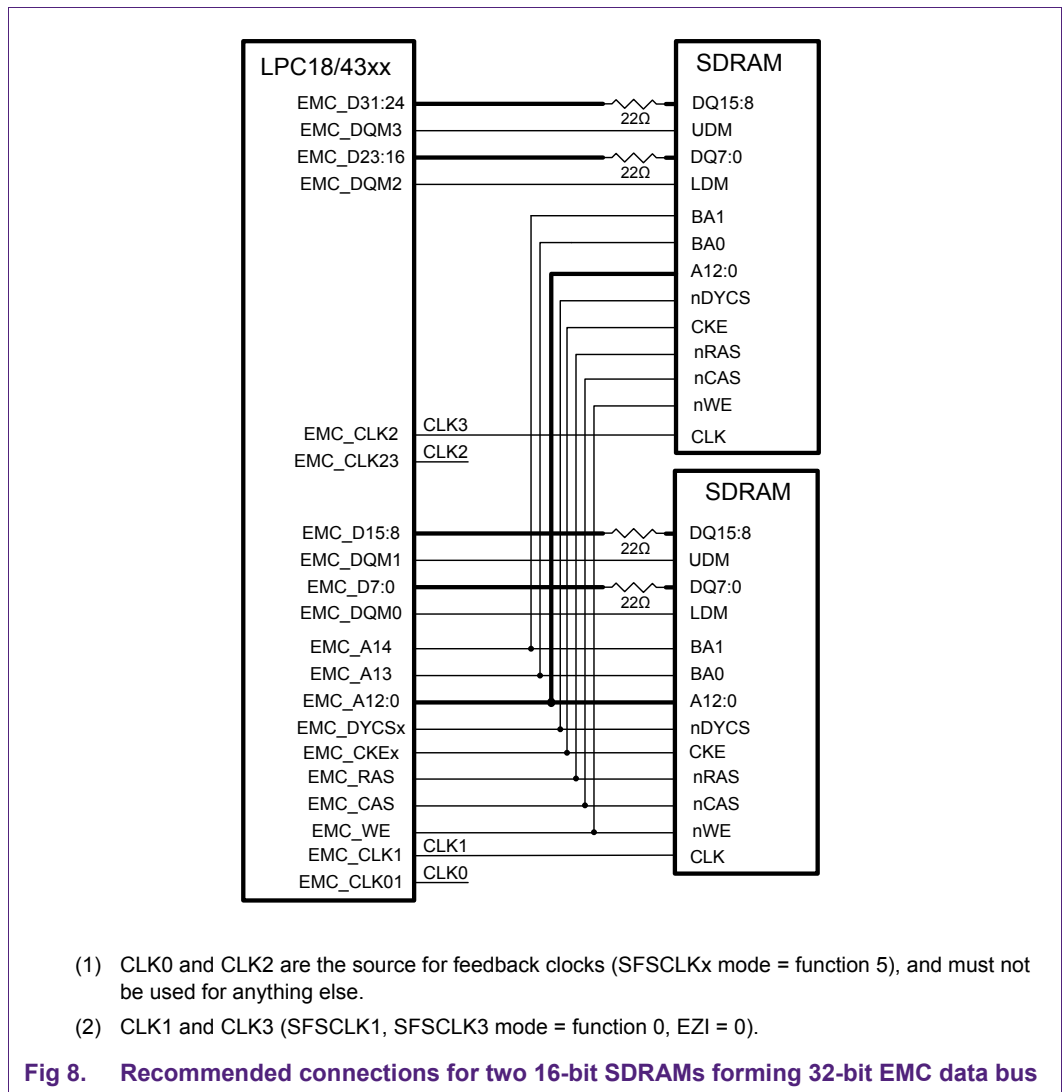
Using a single x32 SDR the maximum memory for each EMC\_DYCS[3:0] is 64 MB (16M x 32). Using two x16 SDRs the maximum memory for each EMC\_DYCS[3:0] is 128 MB (two 32M x 16). Using four x8 SDRs the maximum memory for each EMC\_DYCS[3:1] is 256 MB (four 64M x 8). Using x8 SDRAMs is not recommended, as this is not usually a cost effective configuration, and the higher capacitive loading on the EMC address and control signals, which go to all SDRAMs, may reduce the maximum operational speed of the interface.

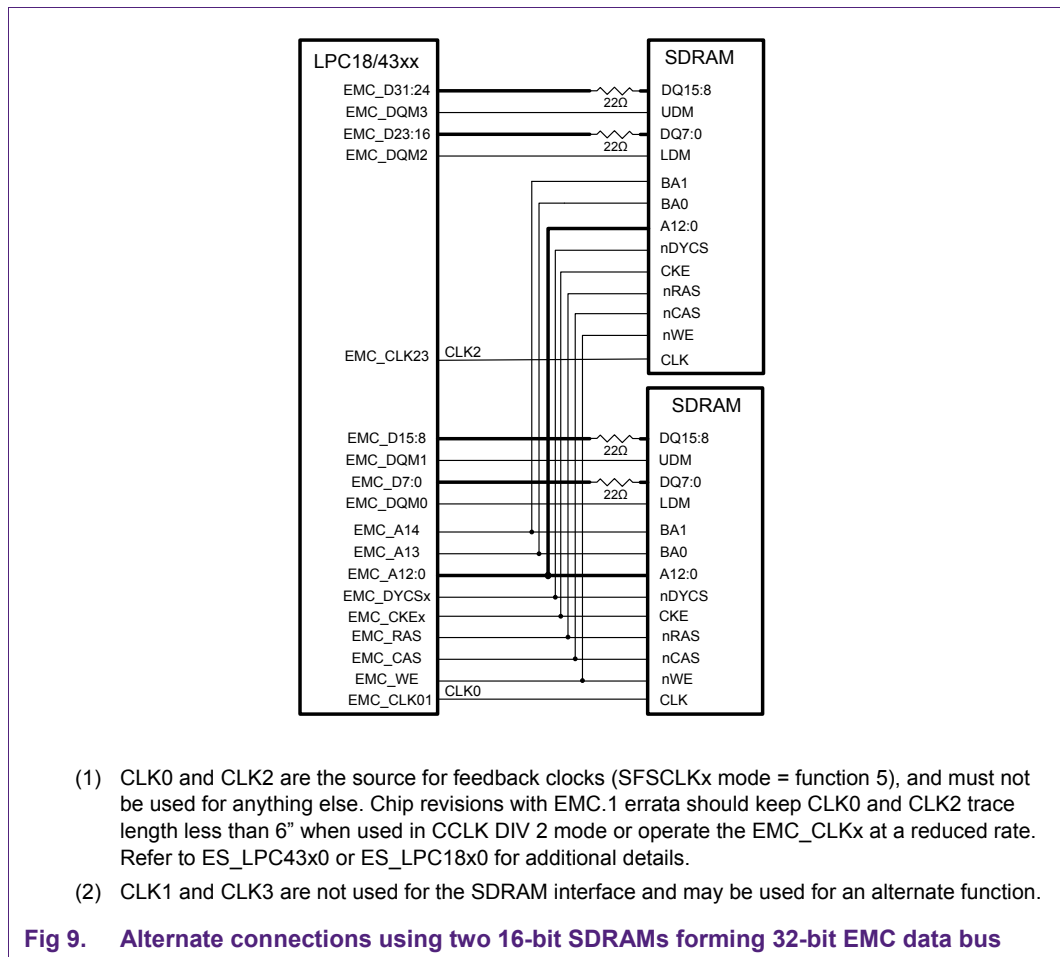
### 2.3.1 Recommended configurations using single DYNCSx

Most applications will require only a single dynamic chip select (DYNCSx). EMC performance may be compromised when PCB traces are longer than 6" or capacitive loads exceed those listed in the datasheet under dynamic characteristics, Dynamic external interface. Using a single SDRAM with either an x16 or x32 data bus will provide minimum loading to the EMC, resulting in maximum EMC performance. The detailed connections using a single x32 SDRAM are shown in Fig 7. When using two x16 SDRAMs to form a 32-bit wide EMC data bus the recommended connections are shown

in Fig 8. An alternate configuration using two x16 SDRAMs, which frees pins CLK1 and CLK3 to be used for other functions, is shown in Fig 9. However, when using the configuration in Fig 9 using chip revisions having EMC.1 errata operating in CCLK DIV2 mode, we recommend limiting CLK0 or CLK2 trace length to no more than 6" or reducing the EMC\_CLKx frequency to less than 102 MHz. Longer CLK0/CLK2 traces result in a lower maximum EMC clock frequency.



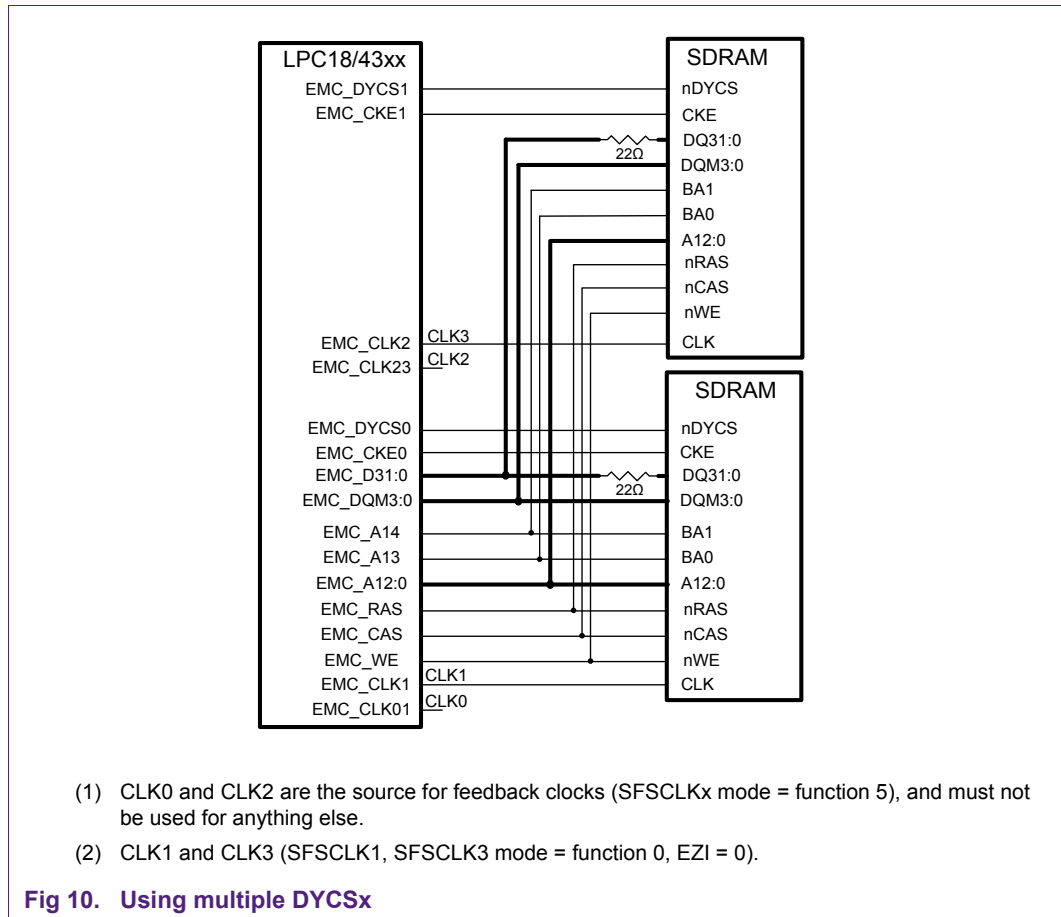




### 2.3.2 Recommended configuration using multiple DYNCSx

When the application requires more external memory capacity than can be supplied by a single 32-bit SDRAM, it is recommended to use x16 or x8 SDRAMs to build a 32-bit EMC data bus on a single DYNCS. This is recommended so the data bus, broken in to byte lanes, only goes to a single SDRAM. However, multiple dynamic chip selects may be used when more system memory is required than can be supported by a single chip select. When using multiple DYNCS, in addition to the address and control signals, the data bus must go to multiple SDRAMs as well. Connecting two 32-bit SDRAMs is shown in [Fig 10](#). An alternate configuration using two x32 SDRAMs which frees pins CLK1 and CLK3 for other functions similar to using two x16 SDRAMs is also possible, but chip revisions with EMC.1 errata should keep CLK0 and CLK2 trace length less than 6" when used in CCLK DIV 2 mode or operate the EMC\_CLKx at a reduced rate. Refer to ES\_LPC43x0 or ES\_LPC18x0 for additional details.





### 2.3.3 Special consideration for EMC pins shared with boot select

Port pins P2\_7, P2\_8, P2\_9, P1\_2 and P1\_1 are used as EMC address signals, and also used for setting the ISPEN (P2\_7) and LPC18/43xx boot mode (P2\_8, P2\_9, P1\_2, P1\_1). The ISPEN and boot mode select signals are generally available at headers, switches, or pull-up/down resistors on the PCB, and they may not be located near the SDRAM. The trick is to isolate the length of trace from the corresponding EMC address bit along the EMC bus from the ISPEN or boot select circuit with a 4.7 kΩ series resistor, as shown in [Fig 11](#).

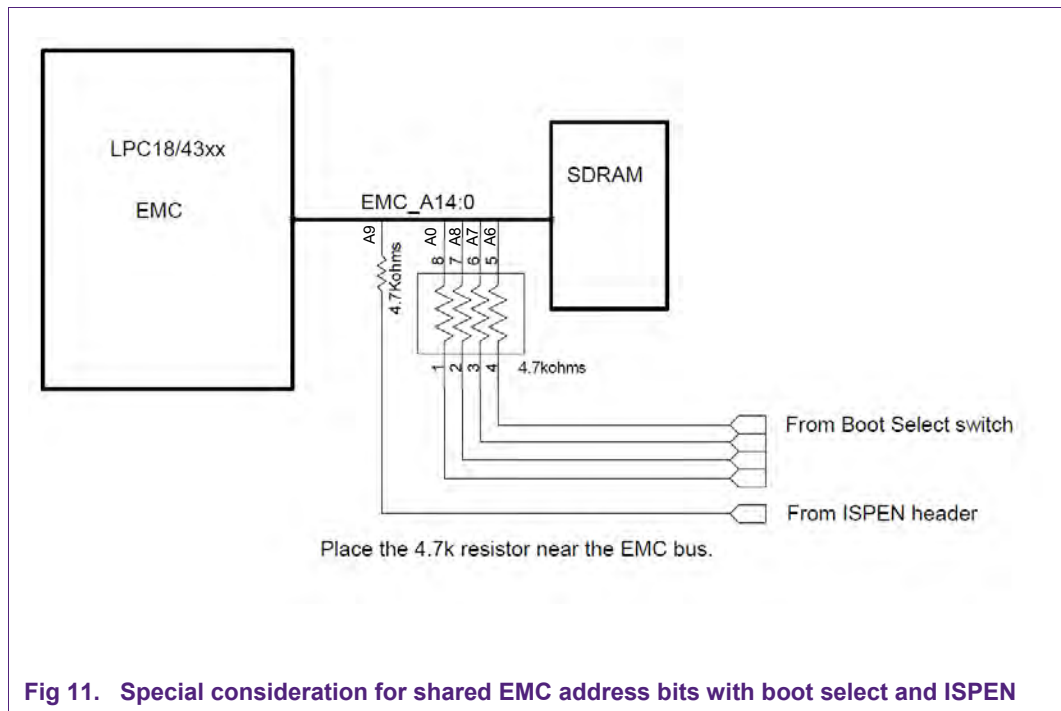


Fig 11. Special consideration for shared EMC address bits with boot select and ISPEN

## 2.4 EMC bus PCB layout topology

EMC CLKx signals should be routed using point-to-point routing topology. When multiple SDRAMs are needed, use one CLKx pin to drive one SDRAM. For a design that requires more than four SDRAMs, each CLKx pin may have two SDRAM clocks connected by a daisy-chain, placing one SDRAM at the end of the daisy-chain and the other no more than 1" from the end of the daisy-chain, keeping any branch stub to 0.5". EMC signals that go to multiple devices, excluding CLKx pins, should be routed in a daisy-chain with branch stubs no longer than 2".

It is possible to route the EMC CLK and other signals in a star topology, but that requires each PCB trace in the star to be length matched to each other, and each PCB trace characteristic impedance be a little more than twice the source impedance of the EMC IO buffer. It is strongly recommended to use star topology routing only after using LPC18xx/43xx and SDRAM Ibis models along with signal integrity software to simulate your design.

### 2.4.1 Shared EMC configuration

The EMC bus can be shared by multiple devices, such as SDRAM, nor-Flash, SRAM or devices with an SRAM-type interface. Below is a list of key items to follow when the design requires EMC bus to be shared.

- Route the EMC bus in a daisy-chain topology.
- In daisy-chain topology place the LPC18xx/43xx at one extreme end of the daisy-chain and the SDRAM at the other extreme end. Other devices can be distributed along the daisy-chain, see [Fig 12](#).
- If more than four devices total (including the SDRAM and LPC18/43xx) are connected to the EMC bus, it is recommended you connect only the SDRAM and bi-directional bus buffers to the LPC18xx/43xx EMC directly, then connect the other devices to the buffered side of the EMC bus, see [Fig 13](#).

- If the EMC is used for SDRAM and expanding connections off the LPC18xx/43xx board, bi-directional bus buffers must be used to isolate the off-board EMC from the SDRAM interface. The SDRAM must be connected directly to the un-buffered EMC bus, see [Fig 13](#). An example of buffering the EMC bus is shown in [Fig 14](#).
- The EMC CLKx routes must be point-to-point. Any test points placed on the CLKx routes should be placed within 1” of the SDRAM. Daisy-chaining two SDRAMs on one CLKx pin is possible, see [section 2.4](#).

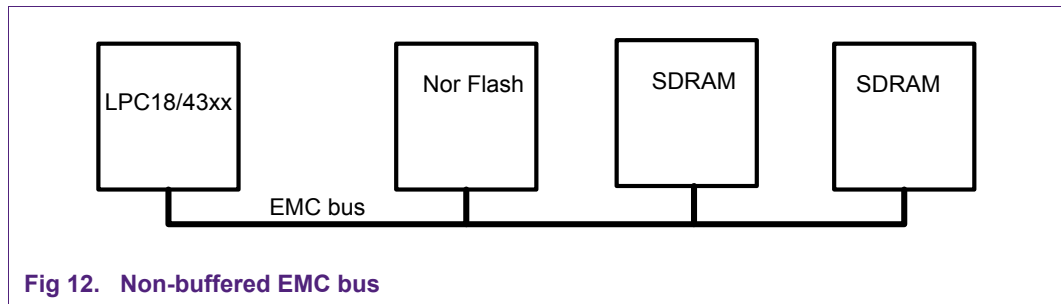


Fig 12. Non-buffered EMC bus

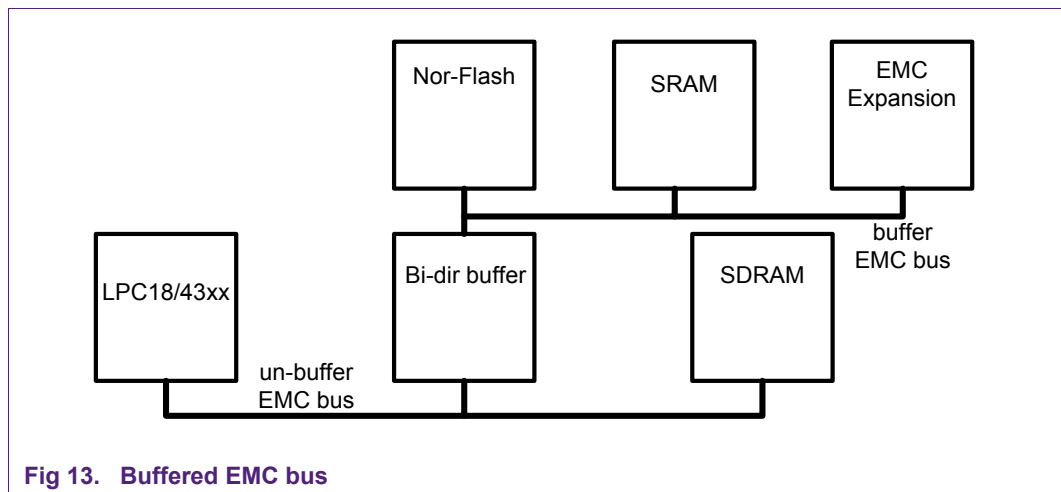
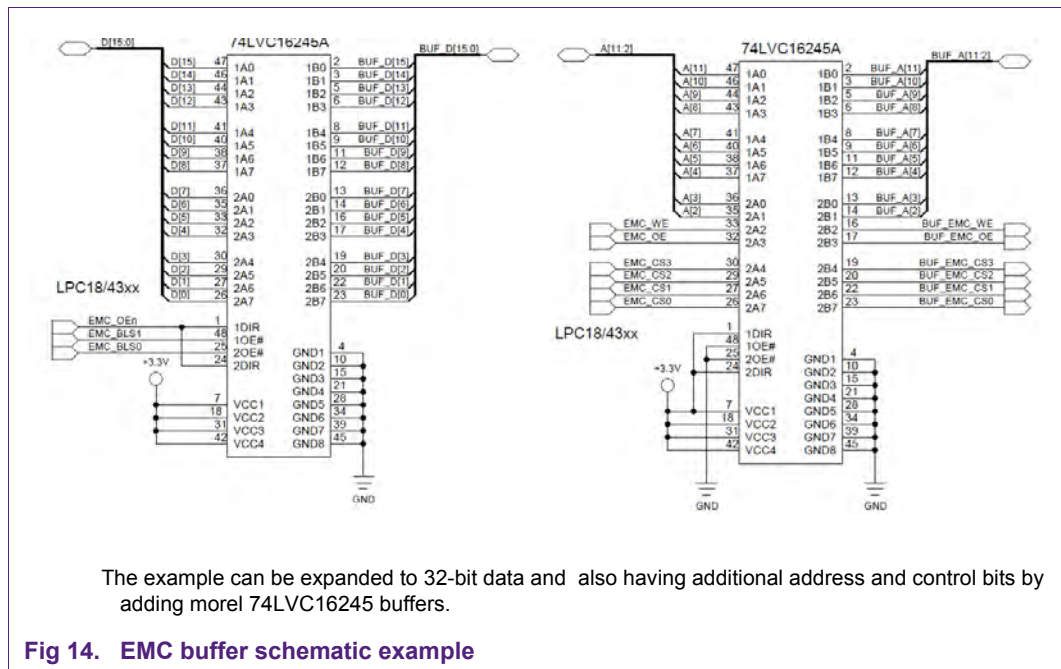


Fig 13. Buffered EMC bus



### 2.5 EMC PCB trace impedance recommendation

The EMC CLKx pins are driven by a high-speed IO buffer. To run the EMC above 75 MHz the LPC18/43xx CLKx pins must be configured for high-speed slew rate (SFSClkx:EHS = 0b1), generating rise / fall times of 350 ps to 700 ps. The CLKx pin source impedance is typically 50 Ω, and matches well to a PCB trace with a characteristic impedance of 60 Ω to 80 Ω without the need for any additional series termination near the LPC18/43xx. All other EMC pins have a normal drive strength buffer output, and must have the slew rate set to fast speed (SPSPx\_x:EHS = 0b1), generating rise / fall times of 1 ns to 2.5 ns. For all EMC pins, other than CLKx, it is recommended to use a PCB trace with a characteristic impedance of 80 Ω to 100 Ω with no external series termination near the EMC pin.

### 2.6 EMC bus terminations

The LPC18xx/43xx EMC IO buffer’s internal source impedance matches well to 60 Ω to 100 Ω PCB trace characteristic impedance. In other words, the series source termination is built-in to the IO buffer, so no termination resistor is needed near the EMC pin.

All single data rate 3 V SDRAM data IO buffers have very strong, low impedance drive strength and no internal drive strength reduction control, resulting in very fast rise and fall times. When the total EMC data bus trace length for any individual data signal is longer than 1.5”, it is recommended that series source termination be placed near the data pins of all SDRAM chips in the design. This will minimize the over-shoot and under-shoot associated with data driven by the SDRAM, also reducing the electro-magnetic interference (EMI) when the SDRAM is driving the EMC data bus.

### 2.7 EMC SDRAM PCB routing rules

Generally, keeping the EMC data bus signals as short as possible and capacitive loading to a minimum is the best practice. Using the rules below as a guide will help ensure proper SDRAM timing is achieved.

Rule 1: At each SDRAM match EMC\_Data[31:0], EMC\_DQM[3:0], EMC\_A[14:0], EMC\_RAS, EMC\_CAS, EMC\_DYCS[3:0]\_N, EMC\_WR\_N, EMC\_CKE[3:0] to within 2" of each other. Since signals require the reflected wave to reach full signal swing, for purposes of the length matching calculation, this is from the LPC18/43xx to the end of the daisy-chain trace (incident wave) plus the distance from the end of the daisy-chain back to the SDRAM pin (reflected wave).

Example calculating effective trace length for matching purposes, reference [Fig 15](#):

Assume Signal 1 length between LPC18/43xx and SDRAM "A" = 3"

Assume Signal 1 length between SDRAM "A" and SDRAM "B" = 2"

Assume Signal 2 length between LPC18/43xx and SDRAM "A" = 2"

Assume Signal 2 length between SDRAM "A" and SDRAM "B" = 2"

The calculation for each signal trace length matching is as follows:

Signal 1 at SDRAM "B" = 3" + 2" = 5"; overall length of the daisy-chain; incident wave.

Signal 2 at SDRAM "B" = 2" + 2" = 4"; overall length of the daisy-chain; incident wave.

Signal 1 at SDRAM "A" = 3" + 2" + 2" = 7"; incident wave + reflected signal back to SDRAM.

Signal 2 at SDRAM "A" = 2" + 2" + 2" = 6"; incident wave + reflected signal back to SDRAM.

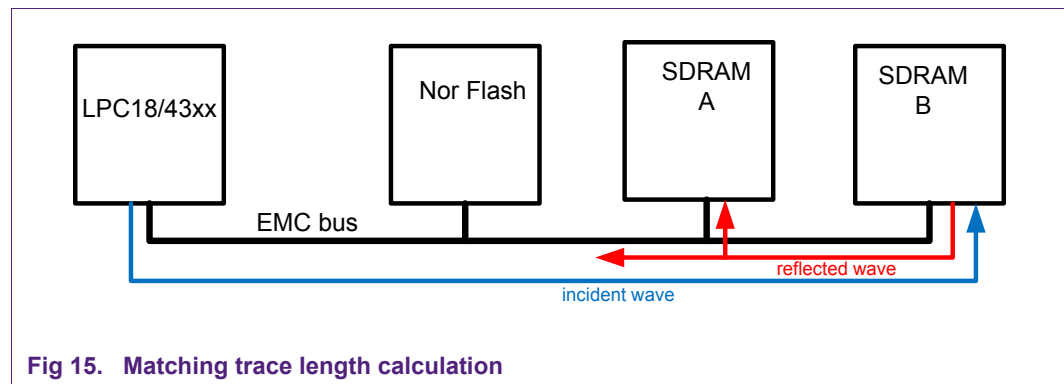


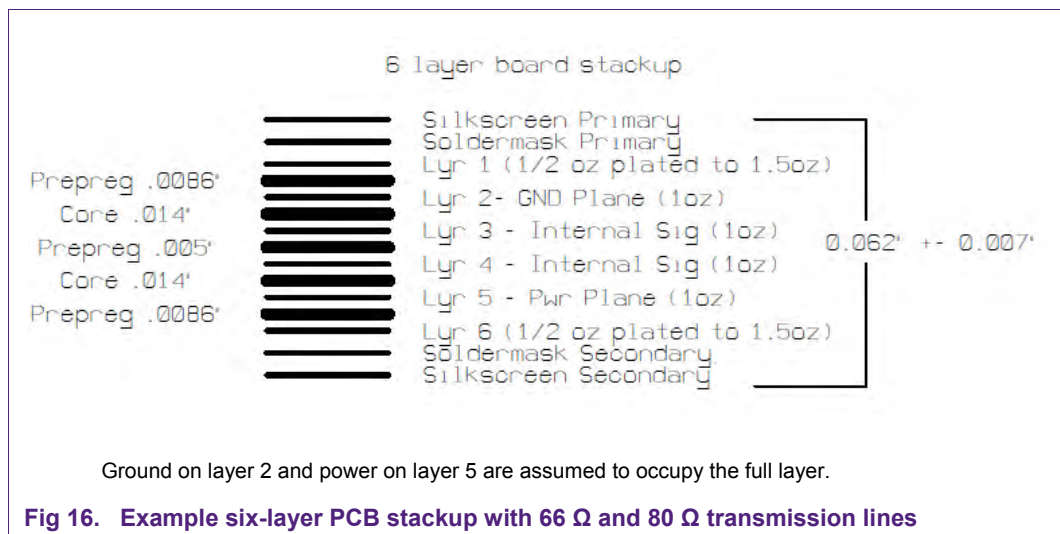
Fig 15. Matching trace length calculation

Rule 2: Any EMC CLKx that's connected to an SDRAM clock should be kept under 6" when also used to provide the feedback clock for SDRAM read data capture, reference [section 2.2.5.1](#). The CLKx trace can be kept short and does not have to match length to other EMC signals. The EMC\_CLKx can be delayed by the EMCDELAYCLK register as necessary to provide the proper SDRAM setup / hold timing, see [section 2.2.2](#).

## 2.8 Example PCB layer stackup

Stackup is a term used to describe the physical arrangement of the layers in a PCB. For any high-speed design the two key elements determined by the stackup are transmission line impedance and inter-plane capacitance. Any board design that uses SDRAM should use a PCB stackup that includes power and ground planes. Pairing each signal layer with an adjacent plane layer (either power or ground) will improve impedance control for each signal layer. The two key dimensional characteristics of the trace affecting impedance value are the height to the nearest plane layer and the trace width. There are sources for

trace impedance calculators available on the internet which can be used to help you get your design near the target trace impedance. However, it's always best to work closely with your board fabrication supplier, and indicate on your supplied board fabrication drawing what nominal impedance value is desired for each trace width which needs to be impedance controlled. Trace impedance and velocity of propagation are also controlled by the dielectric constant of the insulating material used for the PCB. There are a number of materials used for PCB dielectrics, however FR4 is probably the most common low cost dielectric material used for PCBs. An example of a six-layer PCB stackup is shown in Fig 16. The example assumes FR4 (high-tg), having a dielectric constant ( $\epsilon_r$ ) of 4.7, where signal layers 1, 3, 4 and 6 with 0.007" trace width have a nominal characteristic impedance of 65  $\Omega$  to 67  $\Omega$ , and 0.004" trace width have a nominal characteristic impedance of 80  $\Omega$ . One nice thing about this stackup is for any given trace width, no matter which layer it's routed on, the characteristic impedance stays within a couple of ohms. Using the example stackup, all CLKx signals would be routed with 0.007" trace width and all other EMC signals routed with 0.004" width traces. This example is just one of a number of possible six-layer stackups. Again, we recommend you involve your PCB fabrication supplier early in the board design process to assist in selecting dielectric materials, a board stackup and trace widths to meet the desired trace characteristic impedance goals.



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