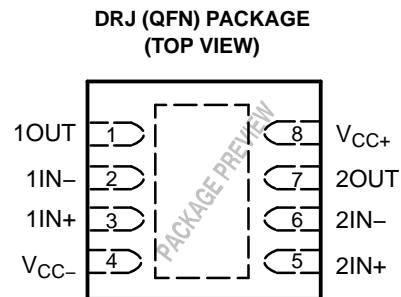
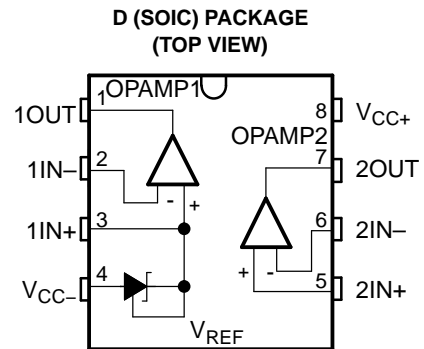


**FEATURES**

- **OPERATIONAL AMPLIFIER**
  - Low Offset Voltage Max of:
    - TL103WA...3 mV (25°C) and 5 mV (Full Temperature)
    - TL103W...4 mV (25°C) and 5 mV (Full Temperature)
  - Low Supply Current...350  $\mu$ A/Channel (Typ)
  - Unity Gain Bandwidth...0.9 MHz (Typ)
  - Input Common-Mode Range Includes GND
  - Large Output-Voltage Swing... 0 V to  $V_{CC} - 1.5$  V
  - Wide Supply-Voltage Range...3 V to 32 V
  - 2-kV ESD Protection (HBM)
- **VOLTAGE REFERENCE**
  - Fixed 2.5-V Reference
  - Tight Tolerance Max of:
    - TL103WA...0.4% (25°C) and 0.8% (Full Temperature)
    - TL103W...0.7% (25°C) and 1.4% (Full Temperature)
  - Low Temperature Drift...7 mV (Typ) Over Operating Temperature Range
  - Wide Sink-Current Range... 0.5 mA (Typ) to 100 mA
  - Output Impedance...0.2  $\Omega$  (Typ)



NOTE: Exposed thermal pad is connected internally to  $V_{CC-}$  via die attach.

**TYPICAL APPLICATIONS**

- Battery Chargers
- Switch-Mode Power Supplies
- Linear Voltage Regulation
- Data-Acquisition Systems

**DESCRIPTION/ORDERING INFORMATION**

The TL103W and TL103WA combine the building blocks of a dual operational amplifier and a fixed voltage reference – both of which often are used in the control circuitry of both switch-mode and linear power supplies. OPAMP1 has its noninverting input internally tied to a fixed 2.5-V reference, while OPAMP2 is independent, with both inputs uncommitted.

For the A grade, especially tight voltage regulation can be achieved through low offset voltages for both operational amplifiers (typically 0.5 mV) and tight tolerances for the voltage reference (0.4% at 25°C and 0.8% over operating temperature range).

The TL103W and TL103WA are characterized for operation from –40°C to 105°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

# TL103W, TL103WA DUAL OPERATIONAL AMPLIFIERS WITH INTERNAL REFERENCE

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## ORDERING INFORMATION

$T_A$	MAX $V_{IO}$ AND $V_{REF}$ TOLERANCE (25°C)	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 105°C	A grade 3 mV, 0.4%	QFN (DRJ)	Reel of 1000	TL103WAIDRJR	PREVIEW
		SOIC (D)	Tube of 75	TL103WAID	Z103WQ
			Reel of 2500	TL103WAIDR	
	Standard grade 4 mV, 0.7%	QFN (DRJ)	Reel of 1000	TL103WIDRJR	PREVIEW
		SOIC (D)	Tube of 75	TL103WID	Z103W
			Reel of 2500	TL103WIDR	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

## Typical Application Circuit

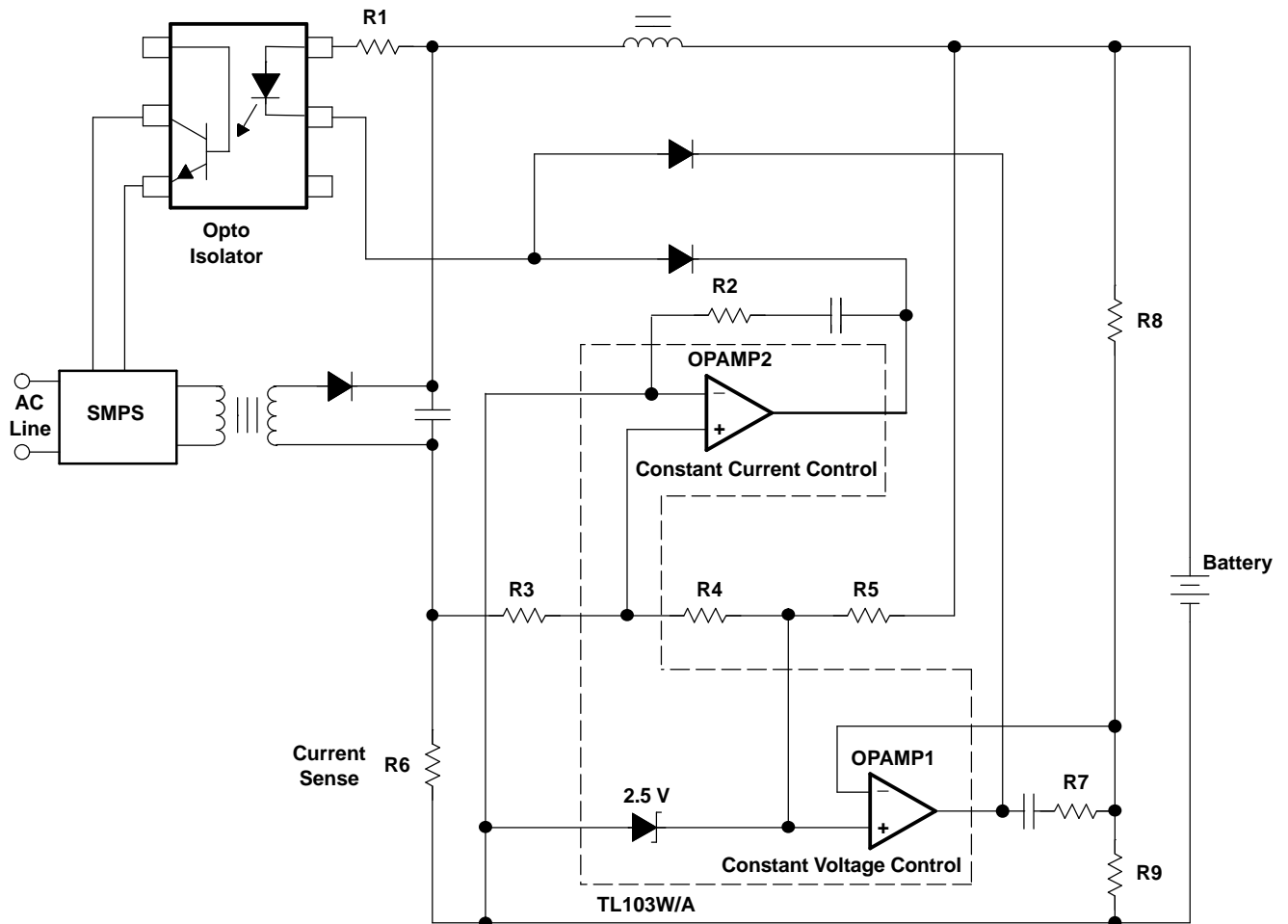


Figure 1. TL103W/A in a Constant-Current and Constant-Voltage Battery Charger

### Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		36	V
V <sub>id</sub>	Operational amplifier input differential voltage		36	V
V <sub>I</sub>	Operational amplifier input voltage range	–0.3	36	V
I <sub>KA</sub>	Voltage reference cathode current		100	mA
θ <sub>JA</sub>	Package thermal impedance		D package <sup>(2)(3)</sup>	97
			DRJ package <sup>(2)(4)</sup>	TBD
T <sub>J</sub>	Maximum junction temperature		150	°C
T <sub>stg</sub>	Storage temperature range	–65	150	°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Maximum power dissipation is a function of T<sub>J</sub>(max), θ<sub>JA</sub>, and T<sub>A</sub>. The maximum allowable power dissipation at any allowable ambient temperature is P<sub>D</sub> = (T<sub>J</sub>(max) – T<sub>A</sub>)/θ<sub>JA</sub>. Selecting the maximum of 150°C can affect reliability.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.
- (4) The package thermal impedance is calculated in accordance with JESD 51-5.

### Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>IN</sub>	Supply voltage	3	32	V
I <sub>K</sub>	Cathode current	1	100	mA
T <sub>A</sub>	Operating free-air temperature	–40	105	°C

# TL103W, TL103WA DUAL OPERATIONAL AMPLIFIERS WITH INTERNAL REFERENCE

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## OPAMP1, Operational Amplifier With Noninverting Input Connected to the Internal $V_{REF}$ Electrical Characteristics

$V_{CC+} = 5\text{ V}$ ,  $V_{CC} = \text{GND}$ ,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A$	MIN	TYP	MAX	UNIT
$V_{IO}$	Input offset voltage	TL103W $V_{icm} = 0\text{ V}$	25°C		1	4	mV
			Full range			5	
	TL103WA $V_{icm} = 0\text{ V}$	25°C		0.5	3		
		Full range			5		
$\alpha V_{IO}$	Input offset-voltage drift		25°C		7	$\mu\text{V}/^\circ\text{C}$	
$I_{IB}$	Input bias current (negative input)		25°C		20	nA	
$A_{VD}$	Large-signal voltage gain	$V_{CC+} = 15\text{ V}$ , $R_L = 2\text{ k}\Omega$ , $V_{icm} = 0\text{ V}$	25°C		100	V/mV	
$k_{SVR}$	Supply-voltage rejection ratio	$V_{CC+} = 5\text{ V}$ to $30\text{ V}$ , $V_{icm} = 0\text{ V}$	25°C	65	100	dB	
$I_{source}$	Output source current	$V_{CC+} = 15\text{ V}$ , $V_O = 2\text{ V}$ , $V_{id} = 1\text{ V}$	25°C	20	40	mA	
$I_{SC}$	Short circuit to GND	$V_{CC+} = 15\text{ V}$	25°C		40	60	mA
$I_{sink}$	Output sink current	$V_{CC+} = 15\text{ V}$ , $V_O = 2\text{ V}$ , $V_{id} = -1\text{ V}$	25°C	10	12		mA
		$V_{CC+} = 15\text{ V}$ , $V_O = 0.2\text{ V}$ , $V_{id} = -1\text{ V}$		12	50		$\mu\text{A}$
$V_{OH}$	High-level output voltage	$V_{CC} = 30\text{ V}$ , $R_L = 2\text{ k}\Omega$	25°C	26	27		V
			Full range	26			
		$V_{CC} = 30\text{ V}$ , $R_L = 10\text{ k}\Omega$	25°C	27	28		
			Full range	27			
$V_{OL}$	Low-level output voltage	$R_L = 10\text{ k}\Omega$	25°C		5	20	mV
			Full range			20	
SR	Slew rate at unity gain	$V_{CC+} = 15\text{ V}$ , $C_L = 100\text{ pF}$ , $R_L = 2\text{ k}\Omega$ , $V_I = 0.5\text{ V}$ to $2\text{ V}$ , unity gain	25°C	0.2	0.4		V/ $\mu\text{s}$
GBW	Gain bandwidth product	$V_{CC+} = 30\text{ V}$ , $V_I = 10\text{ mV}$ , $C_L = 100\text{ pF}$ , $R_L = 2\text{ k}\Omega$ , $f = 100\text{ kHz}$	25°C	0.5	0.9		MHz
THD	Total harmonic distortion	$V_{CC+} = 30\text{ V}$ , $V_O = 2\text{ V}_{pp}$ , $C_L = 100\text{ pF}$ , $R_L = 2\text{ k}\Omega$ , $f = 1\text{ kHz}$ , $A_V = 20\text{ dB}$	25°C		0.02		%

**OPAMP2, Independent Operational Amplifier  
Electrical Characteristics**
 $V_{CC+} = 5\text{ V}$ ,  $V_{CC} = \text{GND}$ ,  $V_O = 1.4\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A$	MIN	TYP	MAX	UNIT
$V_{IO}$	Input offset voltage	TL103W	$V_{icm} = 0\text{ V}$	25°C	1	4	mV
				Full range		5	
		TL103WA	$V_{icm} = 0\text{ V}$	25°C	0.5	3	
				Full range		5	
$\alpha V_{IO}$	Input offset voltage drift		25°C	7		$\mu\text{V}/^\circ\text{C}$	
$I_{IO}$	Input offset current		25°C	2	75	nA	
			Full range		150		
$I_{IB}$	Input bias current		25°C	20	150	nA	
			Full range		200		
$A_{VD}$	Large-signal voltage gain	$V_{CC+} = 15\text{ V}$ , $R_L = 2\text{ k}\Omega$ , $V_O = 1.4\text{ V}$ to $11.4\text{ V}$	25°C	50	100	V/mV	
				Full range	25		
$k_{SVR}$	Supply-voltage rejection ratio	$V_{CC+} = 5\text{ V}$ to $30\text{ V}$	25°C	65	100	dB	
$V_{ICR}$	Input common-mode voltage range	$V_{CC+} = 30\text{ V}^{(1)}$	25°C	0	$V_{CC+} - 1.5$	V	
				Full range	0		$V_{CC+} - 2$
CMRR	Common-mode rejection ratio		25°C	70	85	dB	
			Full range	60			
$I_{source}$	Output source current	$V_{CC+} = 15\text{ V}$ , $V_O = 2\text{ V}$ , $V_{id} = 1\text{ V}$	25°C	20	40	mA	
$I_{SC}$	Short circuit to GND	$V_{CC+} = 15\text{ V}$	25°C	40	60	mA	
$I_{sink}$	Output sink current	$V_{CC+} = 15\text{ V}$ , $V_O = 2\text{ V}$ , $V_{id} = -1\text{ V}$	25°C	10	12	mA	
		$V_{CC+} = 15\text{ V}$ , $V_O = 0.2\text{ V}$ , $V_{id} = -1\text{ V}$		12	50	$\mu\text{A}$	
$V_{OH}$	High-level output voltage	$V_{CC} = 30\text{ V}$ , $R_L = 2\text{ k}\Omega$	25°C	26	27	V	
				Full range	26		
		$V_{CC} = 30\text{ V}$ , $R_L = 10\text{ k}\Omega$	25°C	27	28		
				Full range	27		
$V_{OL}$	Low-level output voltage	$R_L = 10\text{ k}\Omega$	25°C	5	20	mV	
				Full range			20
SR	Slew rate at unity gain	$V_{CC+} = 15\text{ V}$ , $C_L = 100\text{ pF}$ , $R_L = 2\text{ k}\Omega$ , $V_I = 0.5\text{ V}$ to $3\text{ V}$ , unity gain	25°C	0.2	0.4	V/ $\mu\text{s}$	
GBW	Gain bandwidth product	$V_{CC+} = 30\text{ V}$ , $V_I = 10\text{ mV}$ , $C_L = 100\text{ pF}$ , $R_L = 2\text{ k}\Omega$ , $f = 100\text{ kHz}$	25°C	0.5	0.9	MHz	
THD	Total harmonic distortion	$V_{CC+} = 30\text{ V}$ , $V_O = 2\text{ V}_{pp}$ , $C_L = 100\text{ pF}$ , $R_L = 2\text{ k}\Omega$ , $f = 1\text{ kHz}$ , $A_V = 20\text{ dB}$	25°C	0.02		%	
$V_n$	Equivalent input noise voltage	$V_{CC} = 30\text{ V}$ , $R_S = 100\ \Omega$ , $f = 1\text{ kHz}$	25°C	50		$\text{nV}/\sqrt{\text{Hz}}$	

(1) The input common-mode voltage of either input should not be allowed to go below  $-0.3\text{ V}$ . The upper end of the common-mode voltage range is  $V_{CC+} - 1.5\text{ V}$ , but either input can go to  $V_{CC+} + 0.3\text{ V}$  (but  $\leq 36\text{ V}$ ) without damage.

# TL103W, TL103WA DUAL OPERATIONAL AMPLIFIERS WITH INTERNAL REFERENCE

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## Voltage Reference Electrical Characteristics

PARAMETER		TEST CONDITIONS	T <sub>A</sub>	MIN	TYP	MAX	UNIT
V <sub>REF</sub>	Reference voltage	I <sub>K</sub> = 10 mA	25°C	2.482	2.5	2.518	V
			Full range	2.465		2.535	
	TL103WA	I <sub>K</sub> = 10 mA	25°C	2.49	2.5	2.51	
			Full range	2.48		2.52	
ΔV <sub>REF</sub>	Reference input voltage deviation over temperature range	V <sub>KA</sub> = V <sub>REF</sub> , I <sub>K</sub> = 10 mA	Full range		7	30	mV
I <sub>min</sub>	Minimum cathode current for regulation	V <sub>KA</sub> = V <sub>REF</sub>	25°C		0.5	1	mA
z <sub>ka</sub>	Dynamic impedance <sup>(1)</sup>	V <sub>KA</sub> = V <sub>REF</sub> , ΔI <sub>K</sub> = 1 mA to 100 mA, f < 1 kHz	25°C		0.2	0.5	Ω

(1) The dynamic impedance is defined as

$$|z_{ka}| = \frac{\Delta V_{KA}}{\Delta I_K}$$

## Total Device Electrical Characteristics

PARAMETER		TEST CONDITIONS	T <sub>A</sub>	MIN	TYP	MAX	UNIT
I <sub>CC</sub>	Total supply current, excluding cathode-current reference	V <sub>CC+</sub> = 5 V, No load	Full range		0.7	1.2	mA
		V <sub>CC+</sub> = 30 V, No load				2	

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TL103WAID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL103WAIDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL103WAIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL103WAIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL103WAIDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL103WAIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL103WID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL103WIDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL103WIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL103WIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL103WIDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL103WIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

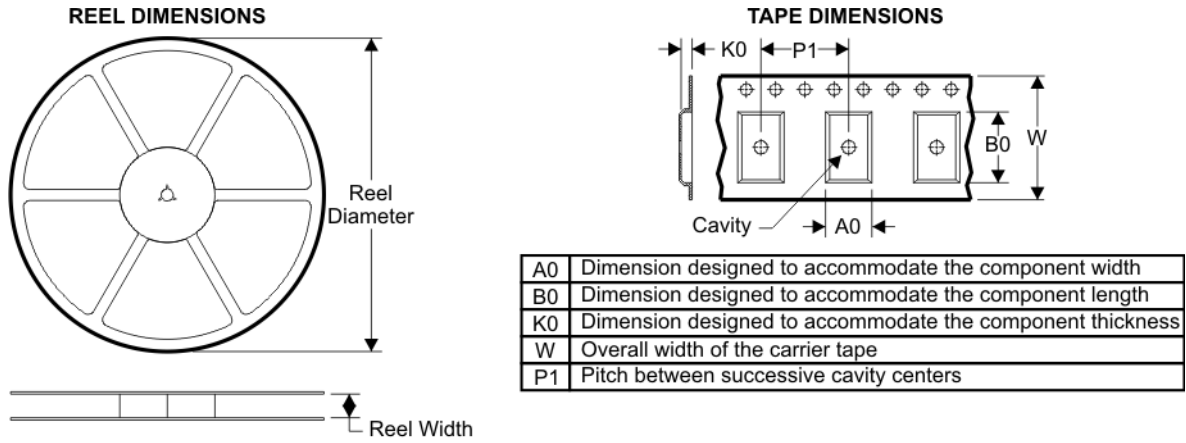
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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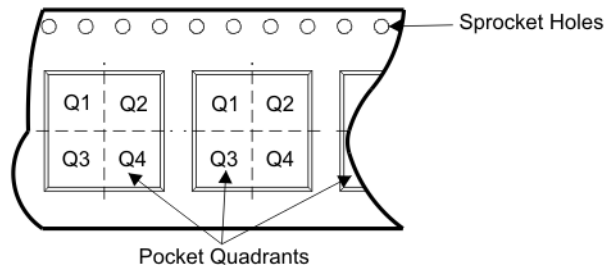
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**TAPE AND REEL BOX INFORMATION**

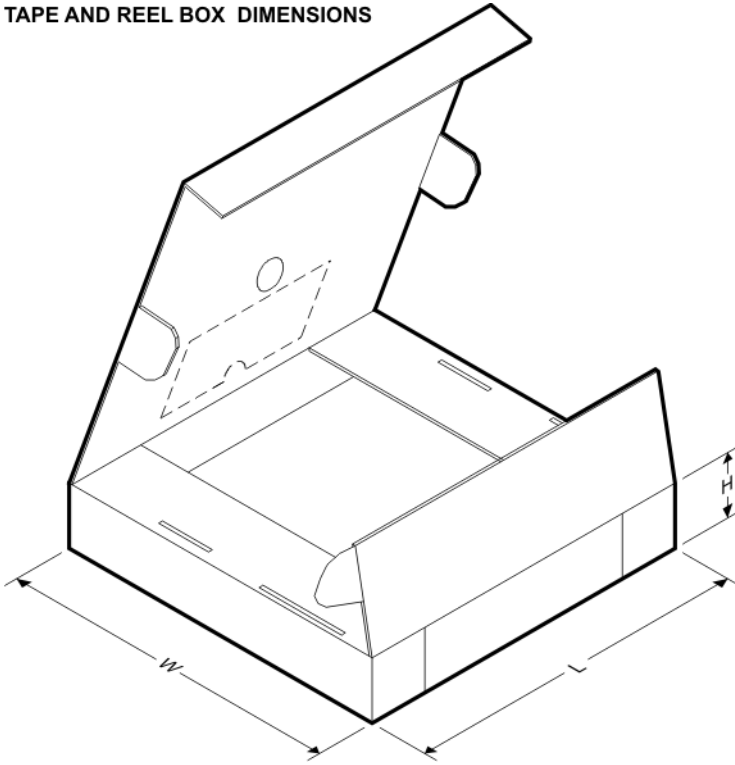


**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL103WAIDR	D	8	SITE 27	330	12	6.4	5.2	2.1	8	12	Q1
TL103WIDR	D	8	SITE 27	330	12	6.4	5.2	2.1	8	12	Q1

**TAPE AND REEL BOX DIMENSIONS**

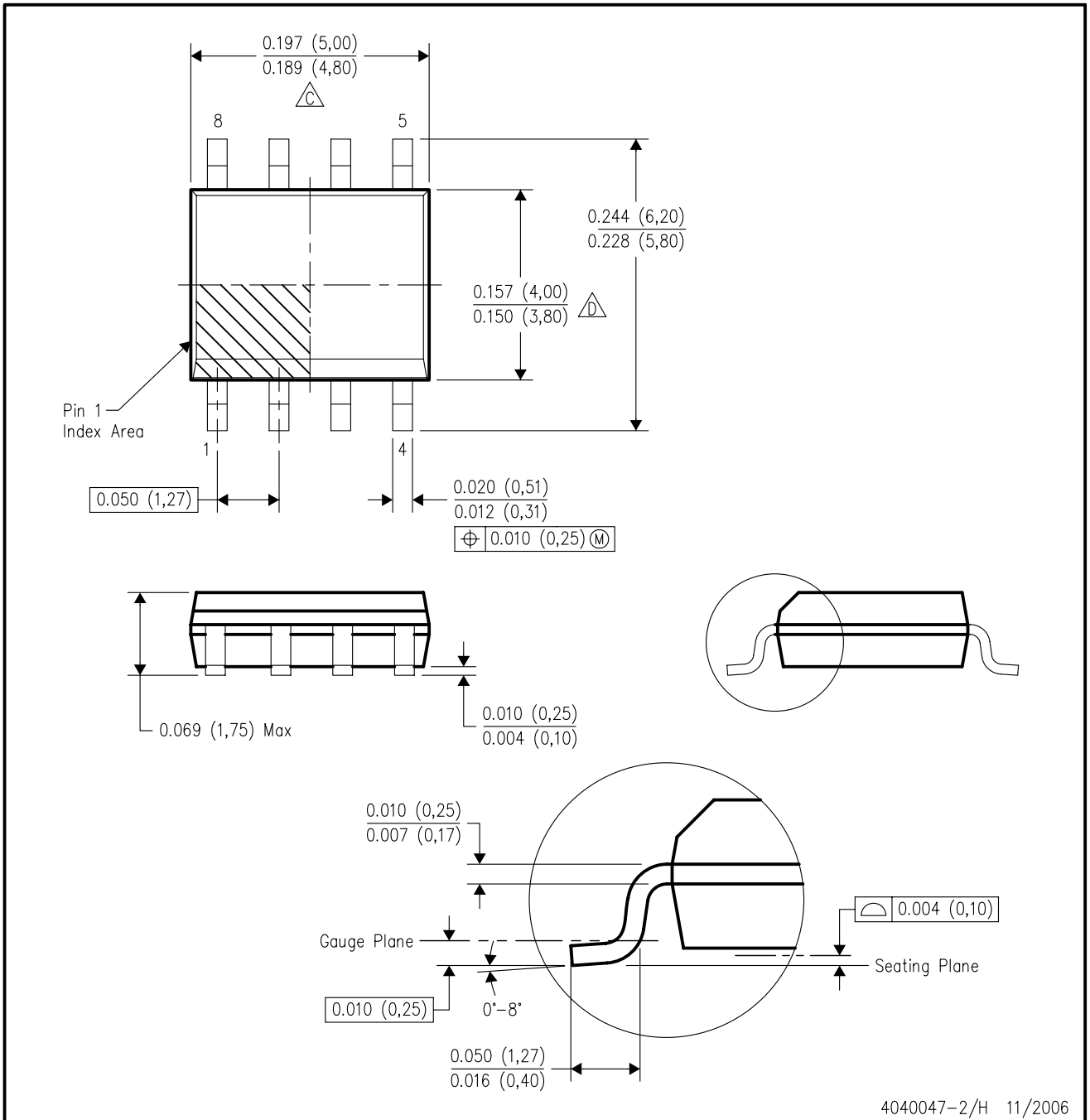


Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
TL103WAIDR	D	8	SITE 27	342.9	338.1	20.64
TL103WIDR	D	8	SITE 27	342.9	338.1	20.64

# MECHANICAL DATA

## D (R-PDSO-G8)

## PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
  - Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
  - Reference JEDEC MS-012 variation AA.

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