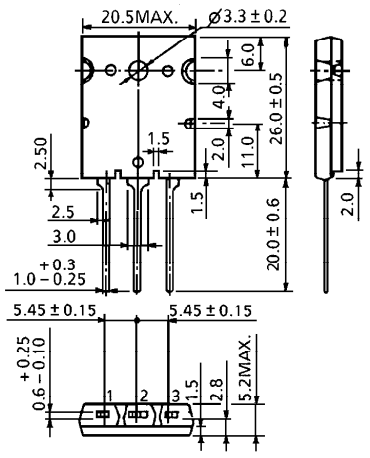
TOSHIBA INSULATED GATE BIPOLAR TRANSISTOR SILICON N-CHANNEL IGBT

GT60M104

HIGH POWER SWITCHING APPLICATIONS

Unit in mm

- High Input Impedance
- High Speed : $t_f = 0.4\mu s$ (Max.)
- Low Saturation Voltage : $V_{CE\,(sat)} = 3.7V$ (Max.)
- Enhancement-Mode
- Recommended FRD S5J12



1. GATE
2. COLLECTOR (HEAT SINK)
3. EMITTER

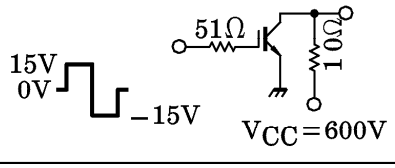
JEDEC	—
EIAJ	—
TOSHIBA	2-21F2C

Weight : 9.75g

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Collector-Emitter Voltage		V_{CES}	900	V
Gate-Emitter Voltage		V_{GES}	±25	V
Collector Current	DC	I_C	60	A
	1ms	I_{CP}	120	
Collector Power Dissipation (Tc = 25°C)		P_C	200	W
Junction Temperature		T_j	150	°C
Storage Temperature Range		T_{stg}	−55~150	°C
Screw Torque		—	0.8	N·m

ELECTRICAL CHARACTERISTICS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Gate Leakage Current		I_{GES}	$V_{GE} = \pm 25V$, $V_{CE} = 0$	—	—	±500	nA
Collector Cut-off Current		I_{CES}	$V_{CE} = 900V$, $V_{GE} = 0$	—	—	1.0	mA
Gate-Emitter Cut-off Voltage		$V_{GE\,(OFF)}$	$I_C = 60mA$, $V_{CE} = 5V$	3.0	—	6.0	V
Collector-Emitter Saturation Voltage		$V_{CE\,(sat)\,(1)}$	$I_C = 10A$, $V_{GE} = 15V$	—	—	2.4	V
		$V_{CE\,(sat)\,(2)}$	$I_C = 60A$, $V_{GE} = 15V$	—	2.4	3.7	
Input Capacitance		C_{ies}	$V_{CE} = 10V$, $V_{GE} = 0$, f = 1MHz	—	5300	—	pF
Switching Time	Rise Time	t_r		—	0.25	0.60	μs
	Turn-on Time	t_{on}		—	0.35	0.80	
	Fall Time	t_f		—	0.25	0.40	
	Turn-off Time	t_{off}		—	0.50	1.00	
Thermal Resistance		$R_{th\,(j-c)}$	—	—	—	0.625	°C / W

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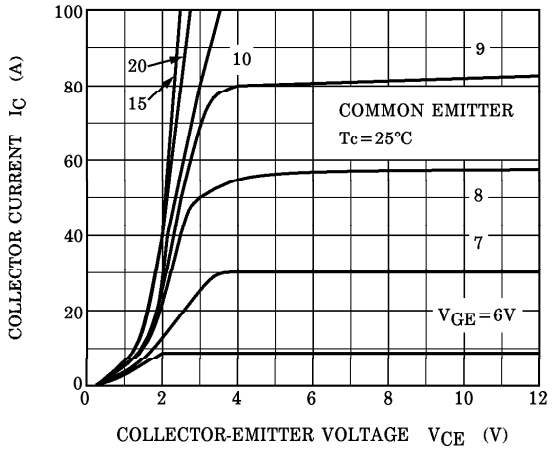
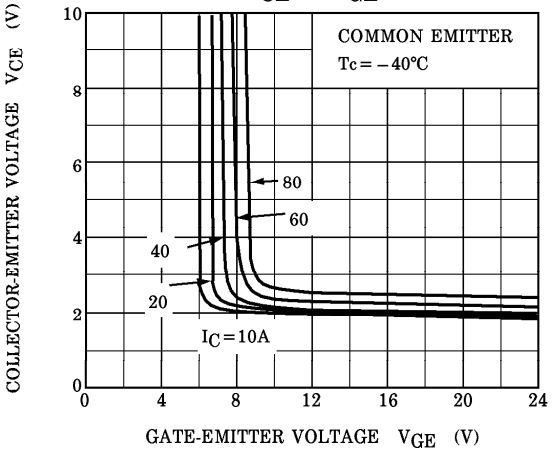
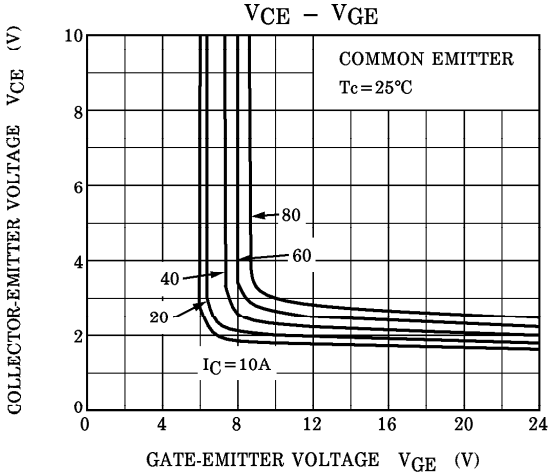
I_C – V_{CE}



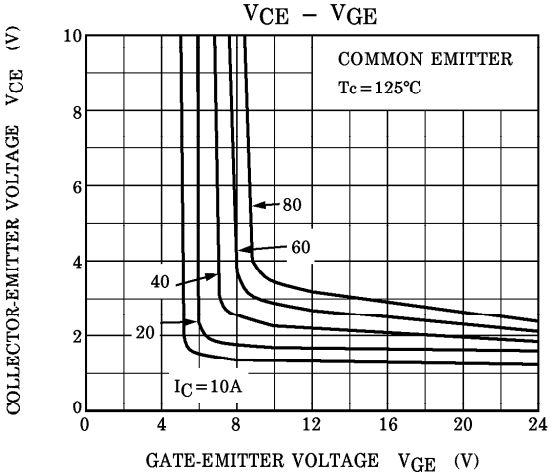
V_{CE} – V_{GE}



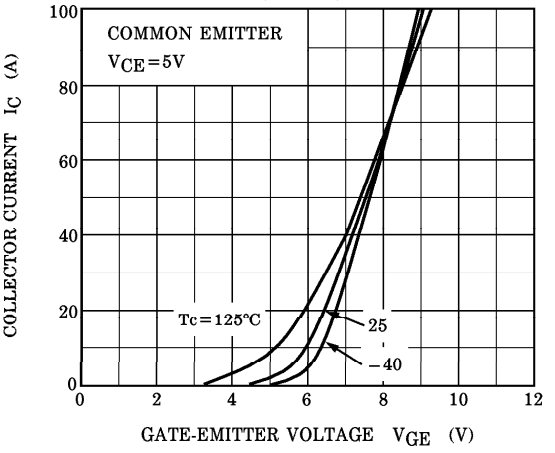
V_{CE} – V_{GE}



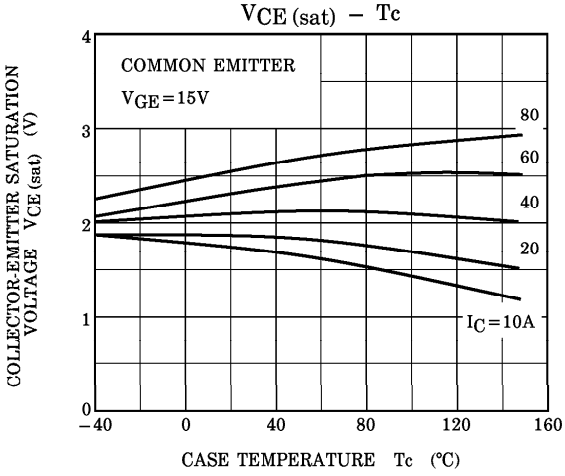
V_{CE} – V_{GE}



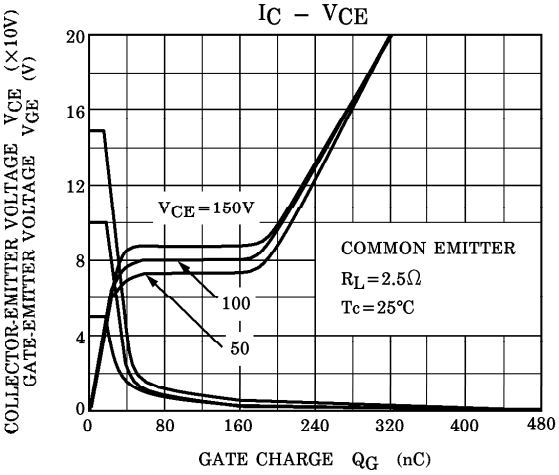
I_C – V_{GE}



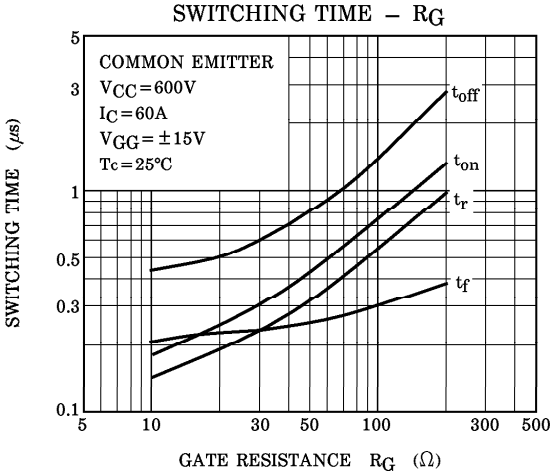
$V_{CE\,(sat)}$ – Tc



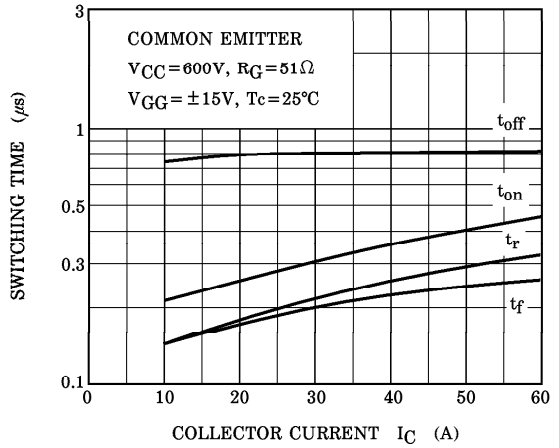
I_C – V_{CE}



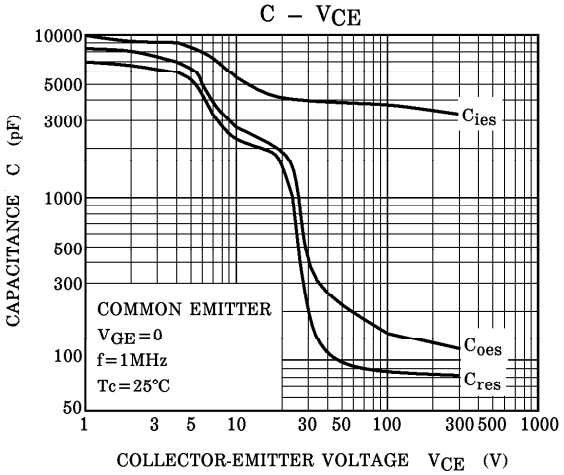
SWITCHING TIME – R_G



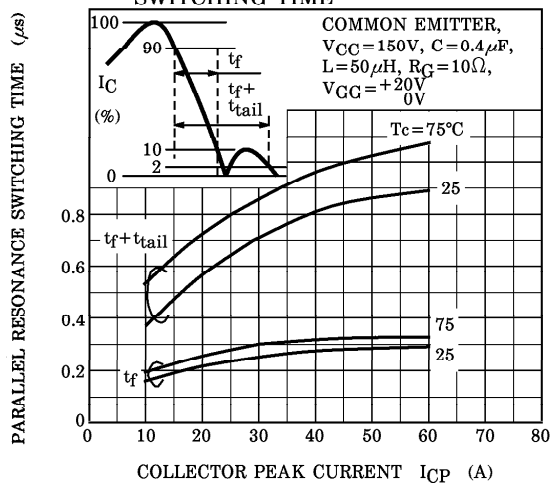
SWITCHING TIME – I_C



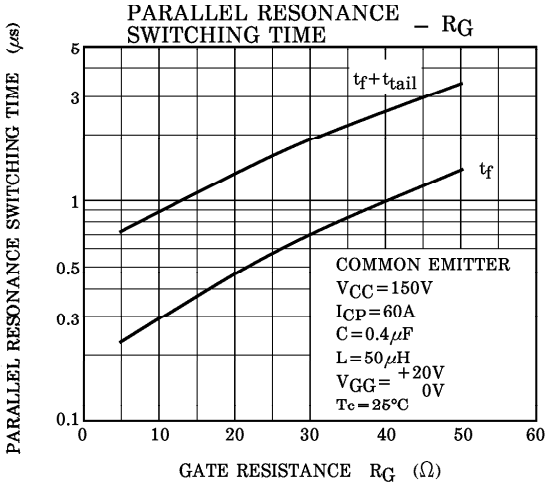
C – V_{CE}



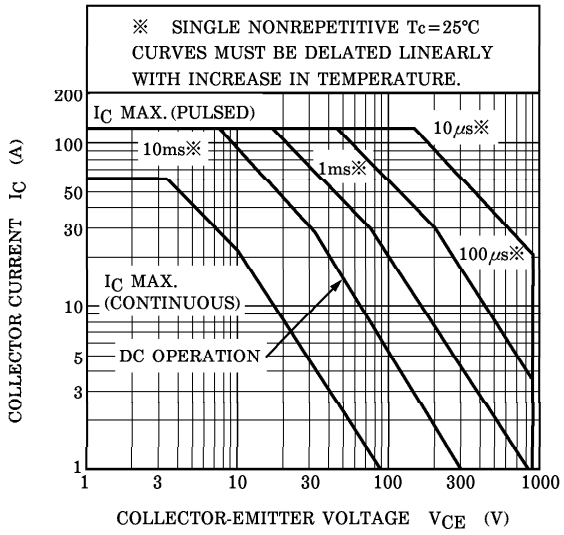
PARALLEL RESONANCE SWITCHING TIME – I_{CP}



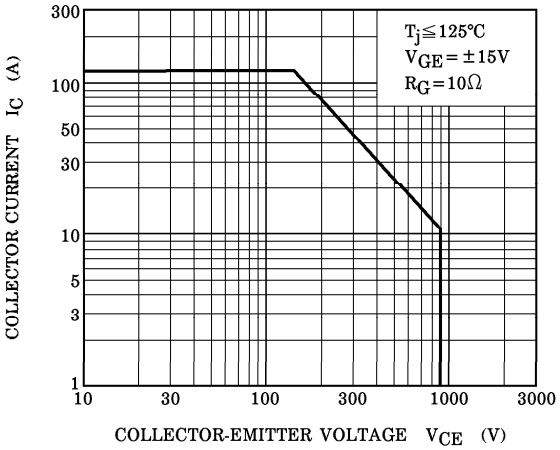
PARALLEL RESONANCE SWITCHING TIME – R_G



SAFE OPERATING AREA



REVERSE BIAS SOA



$R_{th\,(t)}$ – tw