SHARP

LZ244D

Low-Voltage (5 V/12 V) Operation1/4-type
Color CCD Area Sensor with 220k Square Pixels

■ Description

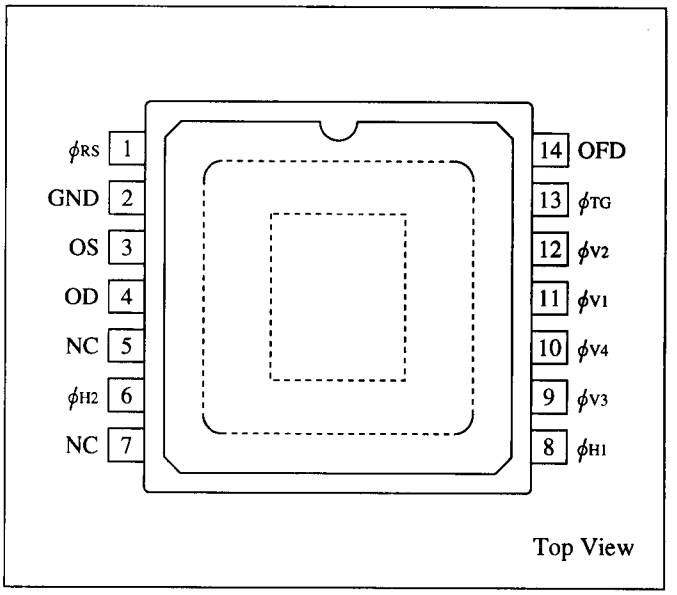
LZ244D is a 1/4-type (4.5 mm) solid state imaging device consisting of PN photo-diodes and CCDs (charge-coupled devices) driven by only positive voltages.

Having about 220 000 pixels (Horizontal 384×Vertical 582), it allows a stable color image to be obtained at high resolution.

■ Features

1. Low-voltage (5 V/12 V) operation
2. Number of video picture elements
   : Horizontal 362×Virtical 582
   Pixel pitch : Horizontal 13.6 μm×Vertical 6.3 μm
   Number of optically black pixel
   : Horizontal; front 2 and rear 20
3. Complementary color filters of Mg, G, Cy, and Ye
4. Built-in overflow drain voltage output circuit, and built-in reset gate bias output circuit
5. Reduced fixed pattern noise and lag
6. No sticking and no image distortion
7. Blooming suppression structure
8. Built-in output amplifier, voltage generator, pulse mix circuit
9. Variable electronic shutter
10. Package
    14-pin WDIP[Plastic](WDIP014-P-0400A)

■ Pin Connections



Top View

■ Pin Description

No.	Symbol	Pin name	Note
1	φ RS	Reset transistor gate clock	1
2	GND	Ground	
3	OS	Video output	
4	OD	Output transistor drain	
5	NC	No connection	
6	φ H2	Horizontal shift resister clock	
7	NC	No connection	
8	φ H1	Horizontal Shift resister clock	
9	φ V3	Vertical shift resister clock	2
10	φ V4	Vertical shift resister clock	
11	φ V1	Vertical shift resister clock	
12	φ V2	Vertical shift resister clock	
13	φ TG	Transfer gate clock	3
14	OFD	Overflow drain	1

Note 1. φ RS, OFD : Use the circuit parameter indicated in "System Configuration Example (P.7)", and do not connect to DC voltage directly.
When not using electrical shutter, connect OFD to GND through a 0.1 μF capacitor and a 1 mΩ resistor.
Note 2. φ V1- φ V4 : Input the clock through a 0.1 μF capacitor.
Note 3. φ TG : Use the circuit parameter indicated in"System Configuration Example (P.7)"

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■ Absolute Maximum Rating

(Ta=25 ℃)

Parameter	Symbol	Rating	Unit	Note
Output transistor drain voltage	V_{OD}	0 to +15	V	
Reset gate clock voltage	$V\phi_{RS}$	(Internal output)	V	1
Vertical shift register clock voltage	$V\phi_{V}$	0 to +7.5	V	
Horizontal shift ragister clock voltage	$V\phi_{H}$	−0.3 to +7.5	V	
Transfer gate clock voltage	$V\phi_{TG}$	−0.3 to +15	V	
Overflow drain voltage	V_{OFD}	(Internal output)	V	2
Storage temperature	T_{stg}	−40 to +85	℃	
Operating ambient temperature	T_{opr}	−20 to +70	℃	

Note 1. Do not connect to DC voltage directly. When ϕ_{RS} is connected to GND, connect V_{OD} to GND. Reset gate clock is applied below 8 Vp-p.

Note 2. Do not connect to DC voltage directly. When OFD is connected to GND, connect V_{OD} to GND. Overflow drain clock is applied below 13 Vp-p.

■ Recommended Operating Conditions

Parameter		Symbol	MIN.	TYP.	MAX.	Unit	Note
Operating ambient temperature		T_{opr}		25		℃	
Output transistor drain voltage		V_{OD}	12	12.5	13	V	
Overflow drain clock	P-P level	$V\phi_{OFD}$	12	12.5	13	V	1
Ground voltage		GND		0		V	
Transfer gate clock	LOW level	$V\phi_{TGL}$	−0.05	0	0.05	V	
	HIGH level	$V\phi_{TGH}$	12	12.5	13	V	
Vertical shift register clock	P-P level	$V\phi_{V1}$, $V\phi_{V2}$, $V\phi_{V3}$, $V\phi_{V4}$	4.7	5.0	5.5	V	2
Horizontal shift register clock	LOW level	$V\phi_{H1L}$, $V\phi_{H2L}$	−0.05	0	0.05	V	
	HIGH level	$V\phi_{H1H}$, $V\phi_{H2H}$	4.7	5.0	5.5	V	
Reset gate clock	P-P level	$V\phi_{RS}$	4.5	5.0	5.5	V	3
Vertical shift register clock frequency		$f\phi_{V1}$, $f\phi_{V2}$, $f\phi_{V3}$, $f\phi_{V4}$		15.63		kHz	
Horizontal shift register clock frequency		$f\phi_{H1}$, $f\phi_{H2}$		6.75		MHz	
Reset gate clock frequency		$f\phi_{RS}$		6.75		MHz	

Note 1. OFD : Use the circuit parameter indicated in "System Configuration Example (P.7)", and do not connect to DC voltage directly.

Note 2. ϕ_{V1} - ϕ_{V4} : Use the circuit parameter indicated in "System Configuration Example (P.7)", and do not connect to DC voltage directly.

Note 3. ϕ_{RS} : Use the circuit parameter indicated in "System Configuration Example (P.7)", and do not connect to DC voltage directly.

※ To apply power, first connect GND and then turn on V_{OD} and then turn on other powers and pulses.
Do not connect the device to or disconnect it from the plug socket while power is being applied.

■ Electrical Characteristics

- Drive method : Field accumulation
- DC and AC conditions : The typical values under the recommended operating conditions.
- Ambient temperature : 25 ℃
- Temperature of light source : 3 200 K
- Infrared absorbing filter (CM-500,1 mm) is used.

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Note
Standard output voltage	V_O		150		mV	2
Photo response non-uniformity	PRNU			15	%	3
Saturation output voltage	V_{sat}	550			mV	4
Dark output voltage	V_{dark}		0.5		mV	1, 5
Dark signal non-uniformity	DSNU		0.5		mV	1, 6
Sensitivity	R		400		mV	7
Smear ratio	SMR		−85		dB	8
Image lag	AI			1.0	%	9
Blooming suppression ratio	ABL	1000				10
Current dissipation	I_{OD}		4.0	8.0	mA	
Output impedance	R_O		400		Ω	
Vector breakup				10	°, %	11
Line crawling				3.0	%	12
Luminance flicker				2.0	%	1, 13

Note 1. Ta=60 ℃

Note 2. The standard output voltage is defined as 150 mV by the average output voltage under uniform illumination.

Note 3. The image area is divided into 10×10 segments. The voltage of a segment is the average of output voltage from all the pixels within the segment.
PRNU is defined by (Vmax−Vmin) / Vo, where Vmax and Vmin are the maximum and the minimum values of each segment's voltage respectively, when the average output voltage Vo is 150 mV.

Note 4. The image area is divided into 10×10 segments. The saturation signal is defined as the minimum of each segment's voltage which is the average of output voltage from all the pixels within the segment, when the exposure level is set as 10 times, compared to standard level.

Note 5. The average output voltage under a non-exposure condition.

Note 6. The image area is divided into 10×10 segments.
DSNU is defined by (Vdmax−Vdmin) under the non-exposure condition where Vdmax and Vdmin are the maximum and the minimum values of each segment's voltage, respectively, that is the average output voltage over all pixels in the segment.

Note 7. The average output voltage when a 1000 lux light source attached with a 90% refrector is imaged by a lens of F4, f50 mm.

Note 8. The sensor is adjusted to position a V/10 square at the center of image area where V is the vertical length of the image area. SMR is defined by the ratio of the output voltage detected during the vertical blanking period to the maximum of the pixel voltage in the V/10 square.

Note 9. The sensor is exposed at the exposure level corresponding to the standard condition preceding non-exposure condition. AI is defined by the ratio between the output voltage measured at the 1st field during the non-exposure period and the standard output voltage.

Note 10. The sensor is adjusted to position a V/10 square at the center of image area.
ABL is the ratio between the exposure at the standard condition and the exposure at a point where a blooming is observed.

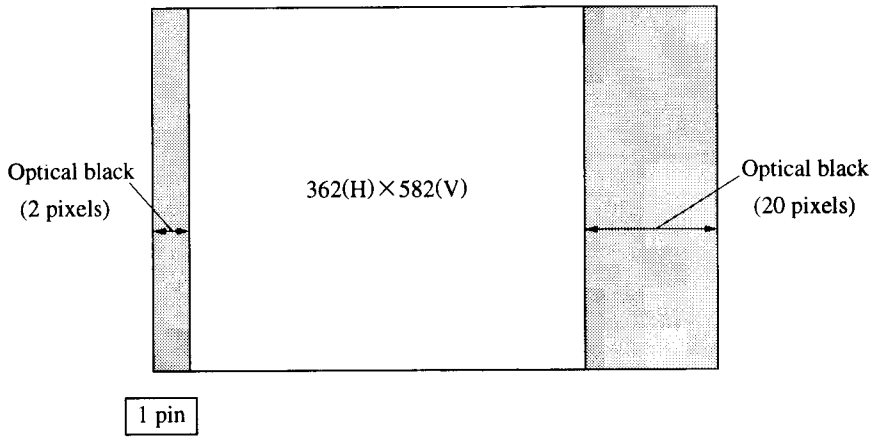
Note 11. Observed with a vector scope when the color bar chart is imaged under the standard exposure condition.

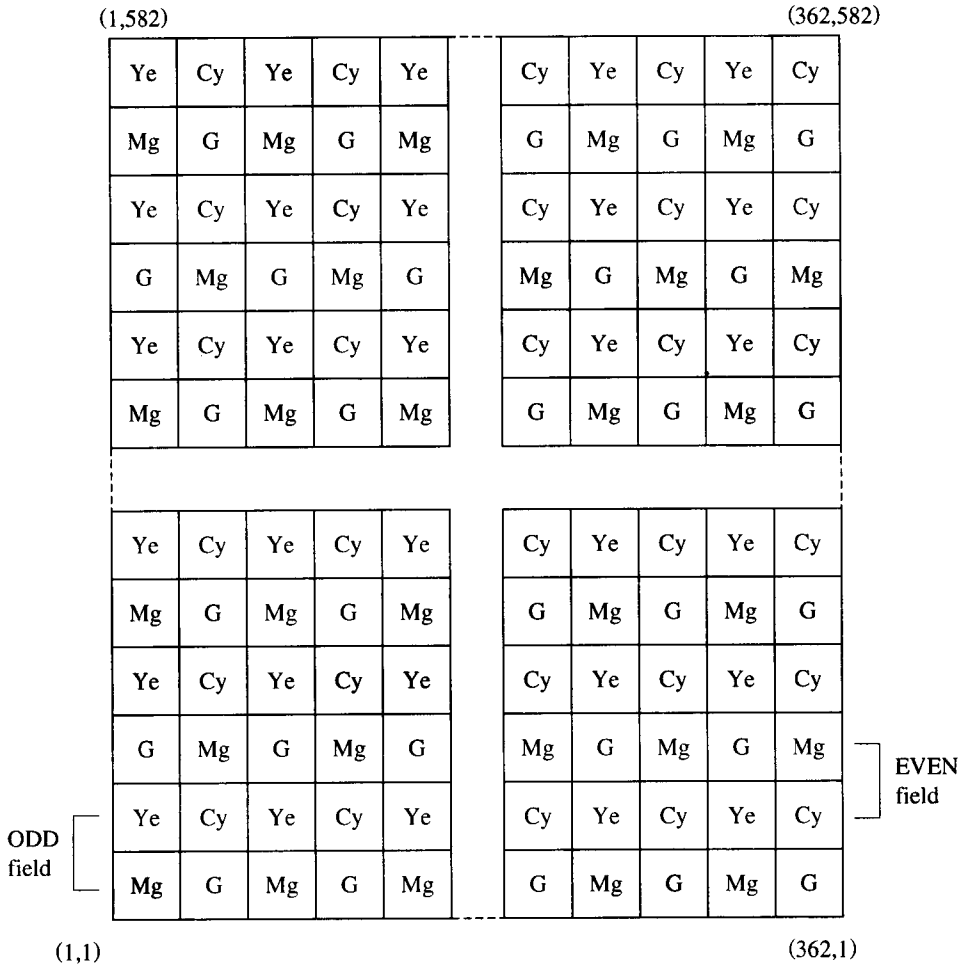
Note 12. The difference between the average output voltage of the (Mg+Ye), (G+Cy) line and the (Mg+Cy), (G+Ye) line under the standard exposure condition.

Note 13. The difference between the average output voltage of the odd field and the even field.

※ Within the recommended operating condition of V_{OD}, V_{OFD} of the internal output satisfy with ABL larger than 1000 times exposure of the standard exposure condition, and Vsat larger than 450 mV.

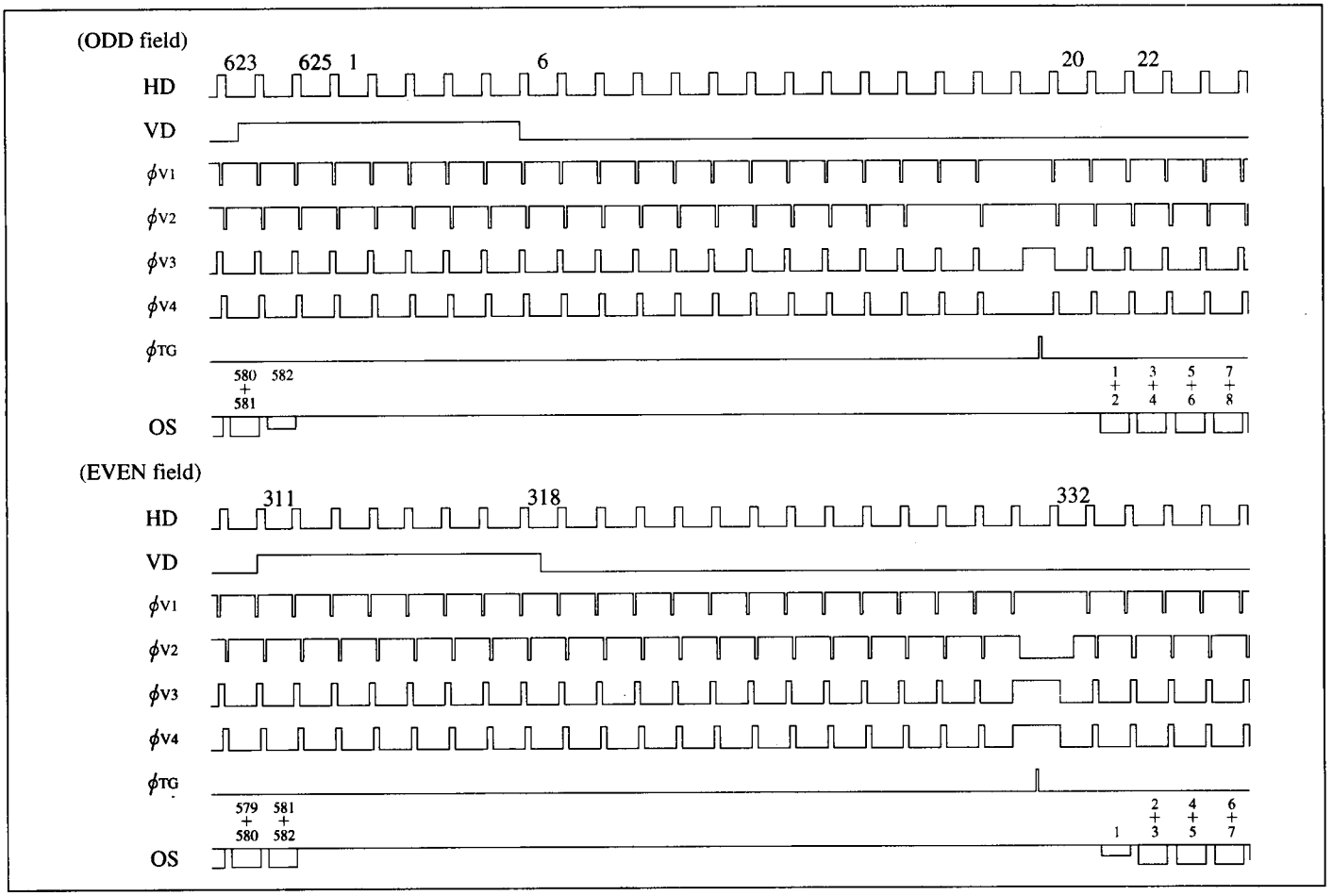
■ Composition of Pixels and Arrangement of Color Filters



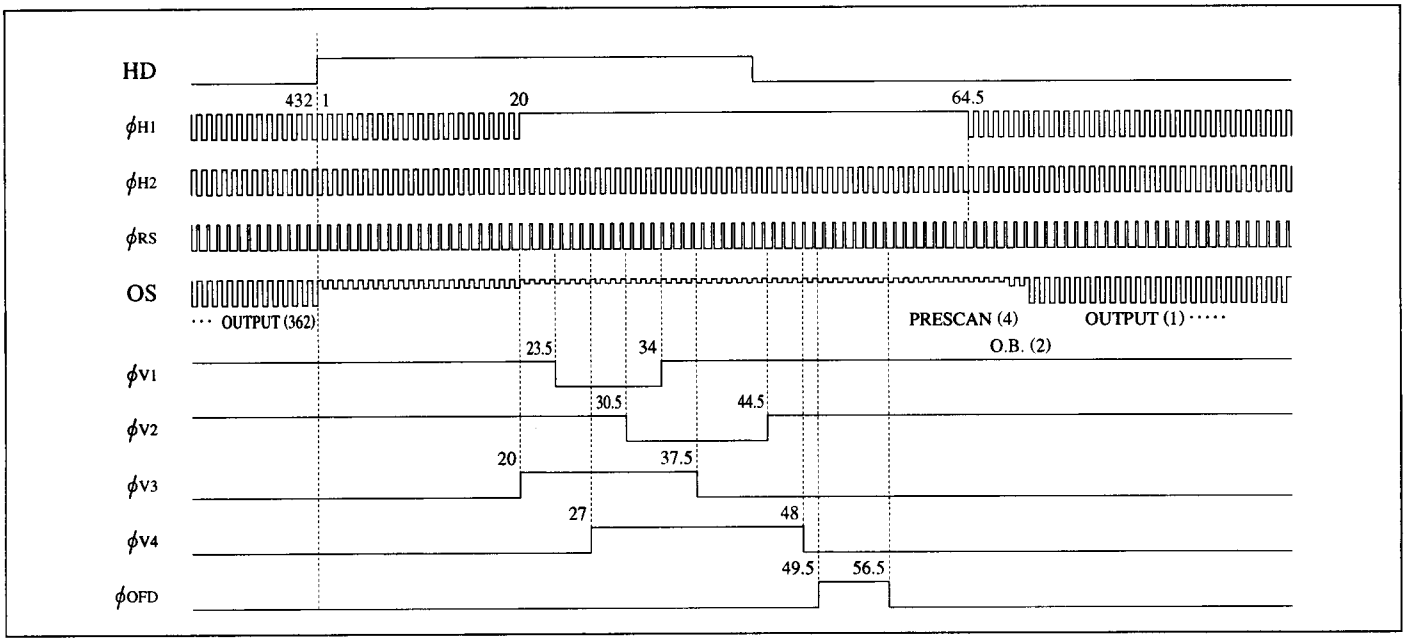


■ Timing Diagram

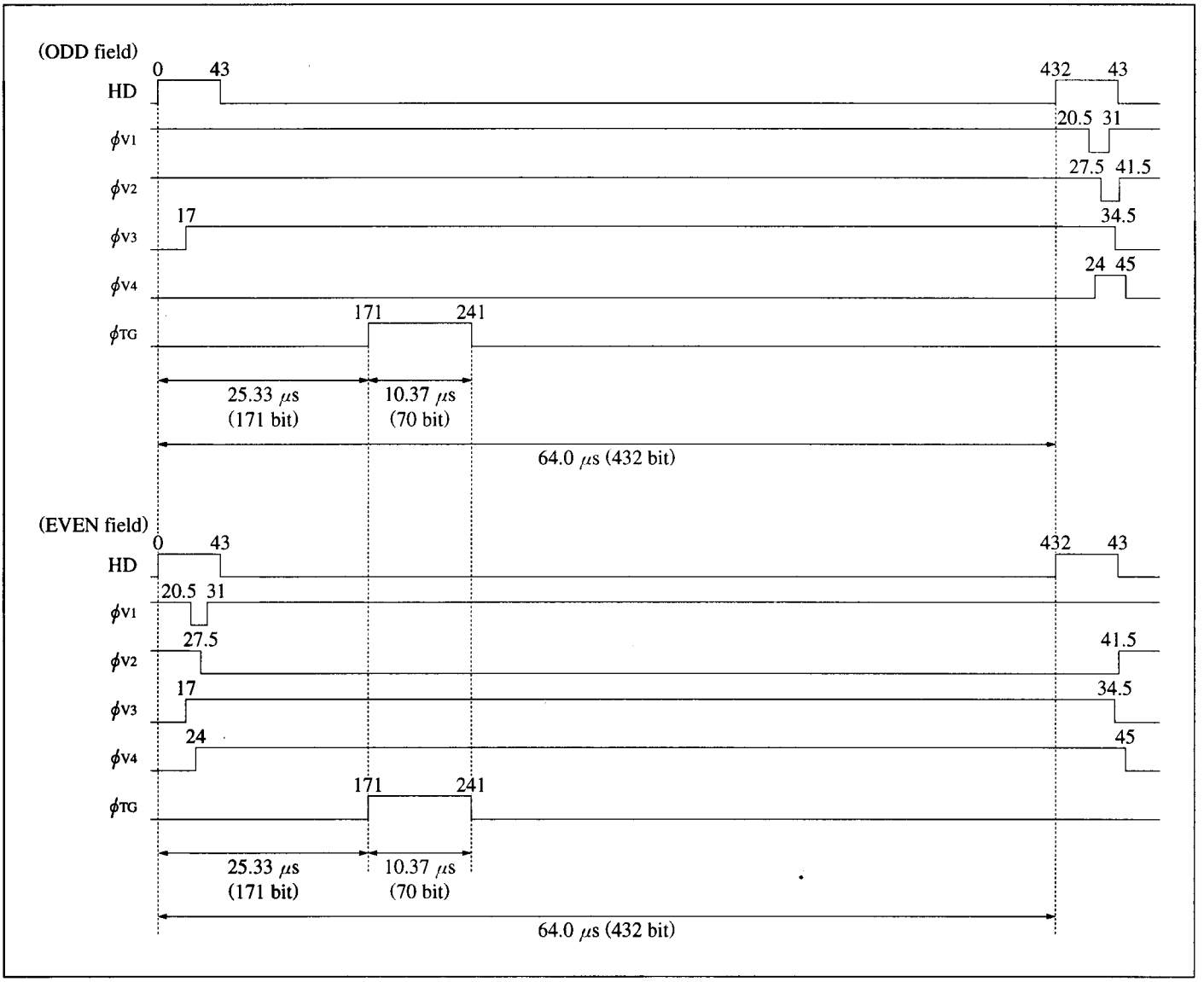
(1) Vertical Transfer Timing



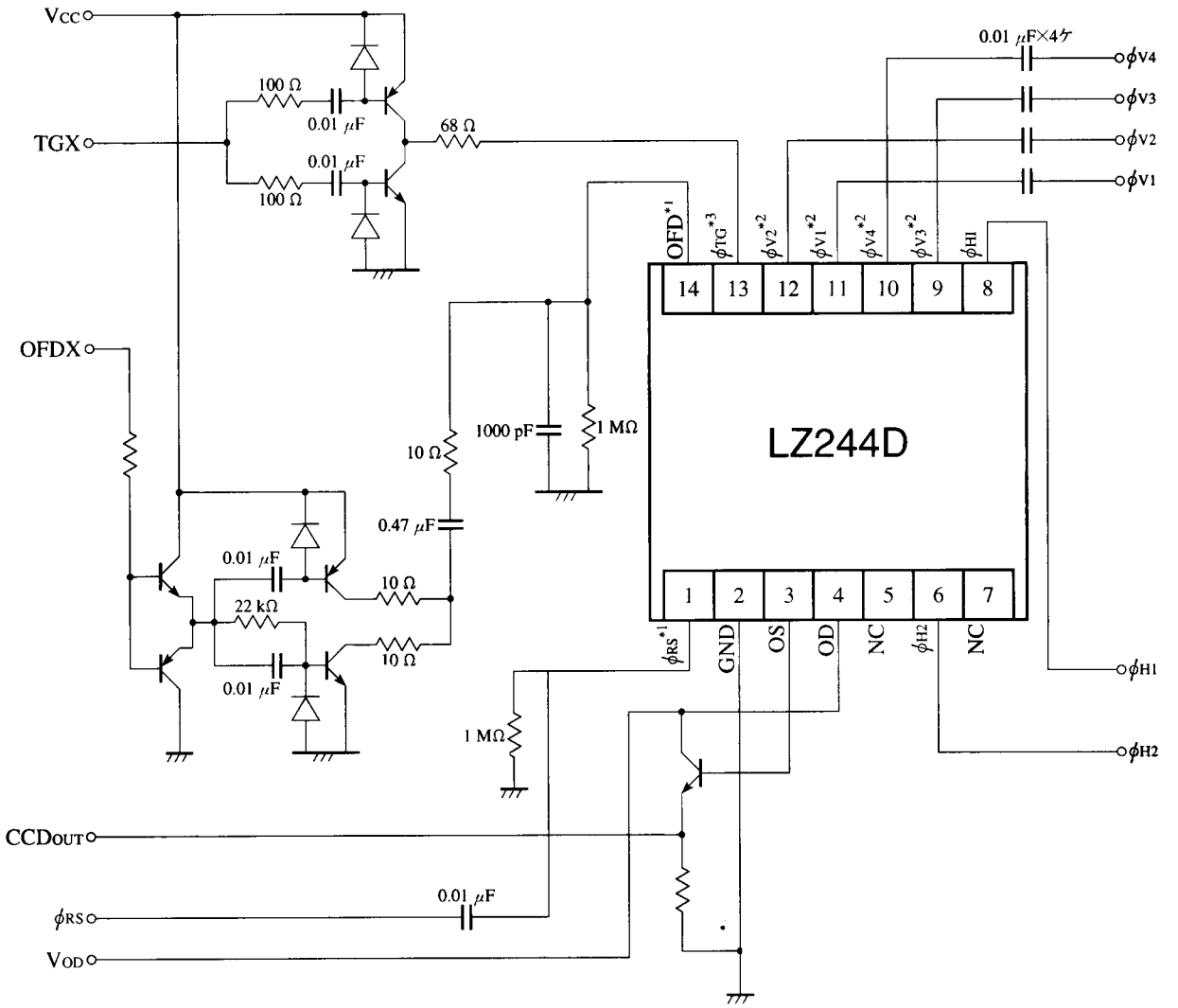
(2) Horizontal Transfer TIming



(3) Read Out Timing



■ System Configuration Example



＊1 φ RS, OFD : Use the circuit parameter indicated in the circuit example, and do not connect to DC voltage directly.
When not using electrical shutter, connect OFD to GND through a 0.1 μF capacitor and a 1 m Ω resistor
＊2 φ V1- φ V4 : Input the clock through a 0.1 μF capacitor.
＊3 φ TG : Use the circuit parameter indicated in the circuit

■ Sharp's Product Line-up (Low-voltage (5 V/12 V) operation 1/4-type CCD Area Sensor)

★Under development

No. of pixels	TV standard		Model No	Electronic shutter (s)	Resolution		Pixels pitch H×V (μm²)	Sensitivity TYP. (mV)	Smear ratio TYP. (%)	Package
					Horizontal TV lines	Effective pixel (H×V)				
220 000	Color	PAL	LZ244D*1	1/80 to 1/10 000	230	362×582	9.4×9.4	400	0.005	14WDIP (Plastic) *3
270 000	Color	NTSC	★LZ2415*2	1/60 to 1/10 000	330	512×492	7.2×5.6	310	0.006	14WDIP (Plastic) *3
	B/W	EIA	LZ2416J*2	1/60 to 1/10 000	380	512×492	7.2×5.6	450	0.006	14WDIP (Plastic) *3
320 000	Color	PAL	★LZ2425*2	1/50 to 1/10 000	330	512×582	7.2×4.7	280	0.006	14WDIP (Plastic) *3
	B/W	CCIR	LZ2426J*2	1/50 to 1/10 000	380	512×582	7.2×4.7	400	0.006	14WDIP (Plastic) *3

＊1 OFD voltage no adjust
＊2 With mirror image function