AN8000/AN8000M Series

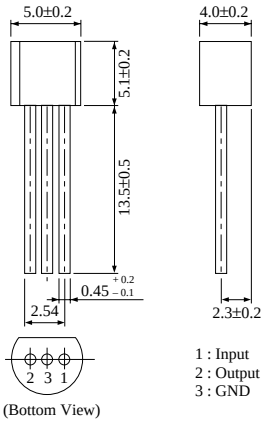
3-pin Positive Output Low Dropout Voltage Regulator (50mA Type)

■ Overview

The AN8000 series is 3-pin low-dropout fixed positive output monolithic voltage regulators. Since thier power consumption can be minimized, they are suitable for battery stabilizing power supply and reference voltage. Thirteen types of output voltage are available ; 2V, 2.5V, 3V, 3.5V (TO-92 only) , 4V, 4.5V, 5V, 6V, 7V, 8V, 8.5V, 9V, and 10V.

AN8000 Series

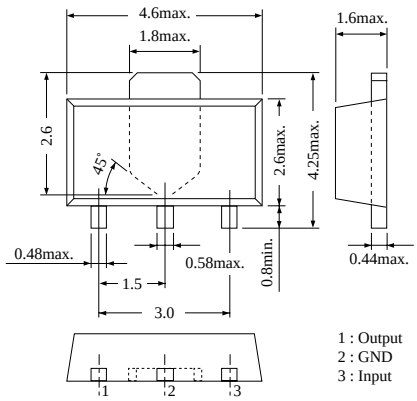
Unit:mm



TO-92 Plastic Package (SSIP003-P-0000)

AN8000M Series

Unit:mm

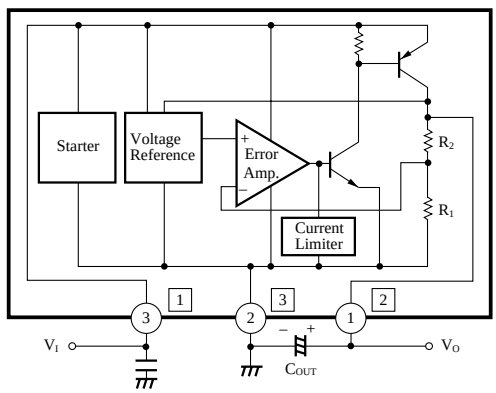


3-pin Mini Power type Plastic Package (TO-243) (HSIP003-P-0000B)

■ Features

- Input/output voltage difference : 0.3V (max.)
- Output current of up to 50mA
- Low bias current ; 0.6mA (typ.)
- Output voltage ; 2V, 2.5V, 3V, 3.5V (TO-92 only) , 4V, 4.5V, 5V, 6V, 7V, 8V, 8.5V, 9V, and 10V.
- Over-voltage protective circuit built-in.

■ Block Diagram



□ : TO-92
○ : TO-243

R_1=5kΩ
C_{IN}=0.33μF
C_{OUT}=10μF

■ Absolute Maximum Ratings (Ta=25˚C)

Parameter		Symbol	Rating	Unit
Supply voltage		V_I	20	V
Supply current		I_{CC}	100	mA
Power dissipation		P_D	650 *	mW
Operating ambient temperature		T_{opr}	–30 to+80	˚C
Storage temperature	AN8000 Series	T_{stg}	–55 to+150	˚C
	AN8000M Series		–55 to+125	

* Mounting onto the PCB (20 × 20 × 1.7mm glass epoxy copper foil 1 cm^2 or more), for AN8000M Series.

■ Electrical Characteristics (Ta=25˚C)

• AN8002/AN8002M (2V Type)

Parameter	Symbol	Condition	min	typ	max	Unit
Output voltage	V_O	T_j=25˚C	1.92	2	2.08	V
Line regulation	REG_{IN}	V_I=2.5 to 8V, T_j=25˚C	—	2	40	mV
Load regulation	REG_L	I_O=1 to 40mA, T_j=25˚C	—	7	20	mV
		I_O=1 to 50mA, T_j=25˚C	—	10	25	mV
Minimum I/O voltage difference	$V_{DIF\ (min.)}$	V_I=1.9V, I_O=20mA, T_j=25˚C	—	0.06	0.2	V
		V_I=1.9V, I_O=50mA, T_j=25˚C	—	0.12	0.3	V
Bias current	I_{bias}	I_O=0mA, T_j=25˚C	—	0.6	1	mA
Ripple rejection ratio	RR	V_I=3 to 5V, f=120Hz	62	74	—	dB
Output noise voltage	V_{no}	f=10Hz to 100kHz	—	60	—	µV
Output voltage temperature coefficient	ΔV_O/Ta	T_j=–30 to+125˚C	—	0.1	—	mV/˚C

Note1) The specified condition T_j=25˚C means that the test should be conducted with each test time reduced (within 10ms) so that the drift in characteristic value due to a temperature rise at chip junction can be ignored.
Note2) Unless otherwise specified, V_I=3V, I_O=20mA, C_O=10µF

• AN8025/AN8025M (2.5V Type)

Parameter	Symbol	Condition	min	typ	max	Unit
Output voltage	V_O	T_j=25˚C	2.4	2.5	2.6	V
Line regulation	REG_{IN}	V_I=3 to 8.5V, T_j=25˚C	—	2.5	50	mV
Load regulation	REG_L	I_O=1 to 40mA, T_j=25˚C	—	8	20	mV
		I_O=1 to 50mA, T_j=25˚C	—	12.5	25	mV
Minimum I/O voltage difference	$V_{DIF\ (min.)}$	V_I=2.4V, I_O=20mA, T_j=25˚C	—	0.07	0.2	V
		V_I=2.4V, I_O=50mA, T_j=25˚C	—	0.12	0.3	V
Bias current	I_{bias}	I_O=0mA, T_j=25˚C	—	0.6	1	mA
Ripple rejection ratio	RR	V_I=3.5 to 5.5V, f=120Hz	60	72	—	dB
Output noise voltage	V_{no}	f=10Hz to 100kHz	—	65	—	µV
Output voltage temperature coefficient	ΔV_O/Ta	T_j=–30 to+125˚C	—	0.13	—	mV/˚C

Note1) The specified condition T_j=25˚C means that the test should be conducted with each test time reduced (within 10ms) so that the drift in characteristic value due to a temperature rise at chip junction can be ignored.
Note2) Unless otherwise specified, V_I=3.5V, I_O=20mA, C_O=10µF

■ Electrical Characteristics (Ta=25˚C)

• AN8003/AN8003M (3V Type)

Parameter	Symbol	Condition	min	typ	max	Unit
Output voltage	V_O	T_j=25˚C	2.88	3	3.12	V
Line regulation	REG_{IN}	V_I=3.5 to 9V, T_j=25˚C	—	3	50	mV
Load regulation	REG_L	I_O=1 to 40mA, T_j=25˚C	—	9	25	mV
		I_O=1 to 50mA, T_j=25˚C	—	15	30	mV
Minimum I/O voltage difference	$V_{DIF\ (min.)}$	V_I=2.9V, I_O=20mA, T_j=25˚C	—	0.07	0.2	V
		V_I=2.9V, I_O=50mA, T_j=25˚C	—	0.12	0.3	V
Bias current	I_{bias}	I_O=0mA, T_j=25˚C	—	0.6	1	mA
Ripple rejection ratio	RR	V_I=4 to 6V, f=120Hz	58	70	—	dB
Output noise voltage	V_{no}	f=10Hz to 100kHz	—	70	—	μV
Output voltage temperature coefficient	$\Delta V_O/Ta$	T_j=–30 to+125˚C	—	0.15	—	mV/˚C

Note1) The specified condition T_j=25˚C means that the test should be conducted with each test time reduced (within 10ms) so that the drift in characteristic value due to a temperature rise at chip junction can be ignored.
Note2) Unless otherwise specified, V_I=4V, I_O=20mA, C_O=10μF

• AN8035/AN8035M (3.5V Type)

Parameter	Symbol	Condition	min	typ	max	Unit
Output voltage	V_O	T_j=25˚C	3.36	3.5	3.64	V
Line regulation	REG_{IN}	V_I=4 to 9.5V, T_j=25˚C	—	3.5	50	mV
Load regulation	REG_L	I_O=1 to 40mA, T_j=25˚C	—	10	30	mV
		I_O=1 to 50mA, T_j=25˚C	—	20	40	mV
Minimum I/O voltage difference	$V_{DIF\ (min.)}$	V_I=3.4V, I_O=20mA, T_j=25˚C	—	0.07	0.2	V
		V_I=3.4V, I_O=50mA, T_j=25˚C	—	0.12	0.3	V
Bias current	I_{bias}	I_O=0mA, T_j=25˚C	—	0.6	1	mA
Ripple rejection ratio	RR	V_I=4.5 to 6.5V, f=120Hz	57	69	—	dB
Output noise voltage	$\mathbf{V_{no}}$	f=10Hz to 100kHz	—	75	—	μV
Output voltage temperature coefficient	$\Delta V_O/Ta$	T_j=–30 to+125˚C	—	0.2	—	mV/˚C

Note1) The specified condition T_j=25˚C means that the test should be conducted with each test time reduced (within 10ms) so that the drift in characteristic value due to a temperature rise at chip junction can be ignored.
Note2) Unless otherwise specified, V_I=4.5V, I_O=20mA, C_O=10μF

• AN8004/AN8004M (4V Type)

Parameter	Symbol	Condition	min	typ	max	Unit
Output voltage	V_O	T_j=25˚C	3.84	4	4.16	V
Line regulation	REG_{IN}	V_I=4.5 to 10V, T_j=25˚C	—	3.5	50	mV
Load regulation	REG_L	I_O=1 to 40mA, T_j=25˚C	—	10	30	mV
		I_O=1 to 50mA, T_j=25˚C	—	20	40	mV
Minimum I/O voltage difference	$V_{DIF\ (min.)}$	V_I=3.8V, I_O=20mA, T_j=25˚C	—	0.07	0.2	V
		V_I=3.8V, I_O=50mA, T_j=25˚C	—	0.12	0.3	V
Bias current	I_{bias}	I_O=0mA, T_j=25˚C	—	0.6	1	mA
Ripple rejection ratio	RR	V_I=5 to 7V, f=120Hz	56	67	—	dB
Output noise voltage	$\mathbf{V_{no}}$	f=10Hz to 100kHz	—	80	—	μV
Output voltage temperature coefficient	$\Delta V_O/Ta$	T_j=–30 to+125˚C	—	0.2	—	mV/˚C

Note1) The specified condition T_j=25˚C means that the test should be conducted with each test time reduced (within 10ms) so that the drift in characteristic value due to a temperature rise at chip junction can be ignored.
Note2) Unless otherwise specified, V_I=5V, I_O=20mA, C_O=10μF

■ Electrical Characteristics (Ta=25˚C)

• AN8045/AN8045M (4.5V Type)

Parameter	Symbol	Condition	min	typ	max	Unit
Output voltage	V_O	T_j=25˚C	4.32	4.5	4.68	V
Line regulation	REG_{IN}	V_I=5 to 10.5V, T_j=25˚C	—	4	50	mV
Load regulation	REG_L	I_O=1 to 40mA, T_j=25˚C	—	11	35	mV
		I_O=1 to 50mA, T_j=25˚C	—	23	45	mV
Minimum I/O voltage difference	$V_{DIF\ (min.)}$	V_I=4.3V, I_O=20mA, T_j=25˚C	—	0.07	0.2	V
		V_I=4.3V, I_O=50mA, T_j=25˚C	—	0.12	0.3	V
Bias current	I_{bias}	I_O=0mA, T_j=25˚C	—	0.7	1	mA
Ripple rejection ratio	RR	V_I=5.5 to 7.5V, f=120Hz	54	66	—	dB
Output noise voltage	V_{no}	f=10Hz to 100kHz	—	85	—	μV
Output voltage temperature coefficient	$\Delta V_O/Ta$	T_j=–30 to+125˚C	—	0.23	—	mV/˚C

Note1) The specified condition T_j=25˚C means that the test should be conducted with each test time reduced (within 10ms) so that the drift in characteristic value due to a temperature rise at chip junction can be ignored.
Note2) Unless otherwise specified, V_I=5.5V, I_O=20mA, C_O=10μF

• AN8005/AN8005M (5V Type)

Parameter	Symbol	Condition	min	typ	max	Unit
Output voltage	V_O	T_j=25˚C	4.8	5	5.2	V
Line regulation	REG_{IN}	V_I=5.5 to 11V, T_j=25˚C	—	4.5	50	mV
Load regulation	REG_L	I_O=1 to 40mA, T_j=25˚C	—	12	40	mV
		I_O=1 to 50mA, T_j=25˚C	—	25	50	mV
Minimum I/O voltage difference	$V_{DIF\ (min.)}$	V_I=4.8V, I_O=20mA, T_j=25˚C	—	0.07	0.2	V
		V_I=4.8V, I_O=50mA, T_j=25˚C	—	0.12	0.3	V
Bias current	I_{bias}	I_O=0mA, T_j=25˚C	—	0.7	1	mA
Ripple rejection ratio	RR	V_I=6 to 8V, f=120Hz	52	64	—	dB
Output noise voltage	V_{no}	f=10Hz to 100kHz	—	95	—	μV
Output voltage temperature coefficient	$\Delta V_O/Ta$	T_j=–30 to+125˚C	—	0.25	—	mV/˚C

Note1) The specified condition T_j=25˚C means that the test should be conducted with each test time reduced (within 10ms) so that the drift in characteristic value due to a temperature rise at chip junction can be ignored.
Note2) Unless otherwise specified, V_I=6V, I_O=20mA, C_O=10μF

• AN8006/AN8006M (6V Type)

Parameter	Symbol	Condition	min	typ	max	Unit
Output voltage	V_O	T_j=25˚C	5.76	6	6.24	V
Line regulation	REG_{IN}	V_I=6.5 to 12V, T_j=25˚C	—	5.5	60	mV
Load regulation	REG_L	I_O=1 to 40mA, T_j=25˚C	—	13	45	mV
		I_O=1 to 50mA, T_j=25˚C	—	28	55	mV
Minimum I/O voltage difference	$V_{DIF\ (min.)}$	V_I=5.8V, I_O=20mA, T_j=25˚C	—	0.07	0.2	V
		V_I=5.8V, I_O=50mA, T_j=25˚C	—	0.13	0.3	V
Bias current	I_{bias}	I_O=0mA, T_j=25˚C	—	0.7	1.2	mA
Ripple rejection ratio	RR	V_I=7 to 9V, f=120Hz	51	63	—	dB
Output noise voltage	V_{no}	f=10Hz to 100kHz	—	105	—	μV
Output voltage temperature coefficient	$\Delta V_O/Ta$	T_j=–30 to+125˚C	—	0.3	—	mV/˚C

Note1) The specified condition T_j=25˚C means that the test should be conducted with each test time reduced (within 10ms) so that the drift in characteristic value due to a temperature rise at chip junction can be ignored.
Note2) Unless otherwise specified, V_I=7V, I_O=20mA, C_O=10μF

■ Electrical Characteristics (Ta=25˚C)

• AN8007/AN8007M (7V Type)

Parameter	Symbol	Condition	min	typ	max	Unit
Output voltage	V_O	T_j=25˚C	6.72	7	7.28	V
Line regulation	REG_{IN}	V_I=7.5 to 13V, T_j=25˚C	—	6.5	70	mV
Load regulation	REG_L	I_O=1 to 40mA, T_j=25˚C	—	14	50	mV
		I_O=1 to 50mA, T_j=25˚C	—	31	60	mV
Minimum I/O voltage difference	$V_{DIF\ (min.)}$	V_I=6.8V, I_O=20mA, T_j=25˚C	—	0.07	0.2	V
		V_I=6.8V, I_O=50mA, T_j=25˚C	—	0.13	0.3	V
Bias current	I_{bias}	I_O=0mA, T_j=25˚C	—	0.7	1.3	mA
Ripple rejection ratio	RR	V_I=8 to 10V, f=120Hz	50	62	—	dB
Output noise voltage	V_{no}	f=10Hz to 100kHz	—	120	—	μV
Output voltage temperature coefficient	$\Delta V_O/Ta$	T_j=–30 to+125˚C	—	0.35	—	mV/˚C

Note1) The specified condition T_j=25˚C means that the test should be conducted with each test time reduced (within 10ms) so that the drift in characteristic value due to a temperature rise at chip junction can be ignored.
Note2) Unless otherwise specified, V_I=8V, I_O=20mA, C_O=10μF

• AN8008/AN8008M (8V Type)

Parameter	Symbol	Condition	min	typ	max	Unit
Output voltage	V_O	T_j=25˚C	7.68	8	8.32	V
Line regulation	REG_{IN}	V_I=8.5 to 14V, T_j=25˚C	—	7.5	80	mV
Load regulation	REG_L	I_O=1 to 40mA, T_j=25˚C	—	15	55	mV
		I_O=1 to 50mA, T_j=25˚C	—	34	65	mV
Minimum I/O voltage difference	$V_{DIF\ (min.)}$	V_I=7.8V, I_O=20mA, T_j=25˚C	—	0.07	0.2	V
		V_I=7.8V, I_O=50mA, T_j=25˚C	—	0.14	0.3	V
Bias current	I_{bias}	I_O=0mA, T_j=25˚C	—	0.7	1.3	mA
Ripple rejection ratio	RR	V_I=9 to 11V, f=120Hz	49	61	—	dB
Output noise voltage	V_{no}	f=10Hz to 100kHz	—	135	—	μV
Output voltage temperature coefficient	$\Delta V_O/Ta$	T_j=–30 to+125˚C	—	0.4	—	mV/˚C

Note1) The specified condition T_j=25˚C means that the test should be conducted with each test time reduced (within 10ms) so that the drift in characteristic value due to a temperature rise at chip junction can be ignored.
Note2) Unless otherwise specified, V_I=9V, I_O=20mA, C_O=10μF

• AN8085/AN8085M (8.5V Type)

Parameter	Symbol	Condition	min	typ	max	Unit
Output voltage	V_O	T_j=25˚C	8.16	8.50	8.84	V
Line regulation	REG_{IN}	V_I=9 to 14.5V, T_j=25˚C	—	8.3	90	mV
Load regulation	REG_L	I_O=1 to 40mA, T_j=25˚C	—	16	60	mV
		I_O=1 to 50mA, T_j=25˚C	—	36	70	mV
Minimum I/O voltage difference	$V_{DIF\ (min.)}$	V_I=8.3V, I_O=20mA, T_j=25˚C	—	0.07	0.2	V
		V_I=8.3V, I_O=50mA, T_j=25˚C	—	0.14	0.3	V
Bias current	I_{bias}	I_O=0mA, T_j=25˚C	—	0.8	1.4	mA
Ripple rejection ratio	RR	V_I=9.5 to 11.5V, f=120Hz	48	60	—	dB
Output noise voltage	V_{no}	f=10Hz to 100kHz	—	140	—	μV
Output voltage temperature coefficient	$\Delta V_O/Ta$	T_j=–30 to+125˚C	—	0.43	—	mV/˚C

Note1) The specified condition T_j=25˚C means that the test should be conducted with each test time reduced (within 10ms) so that the drift in characteristic value due to a temperature rise at chip junction can be ignored.
Note2) Unless otherwise specified, V_I=9.5V, I_O=20mA, C_O=10μF

■ Electrical Characteristics (Ta=25˚C)

• AN8009/AN8009M (9V Type)

Parameter	Symbol	Condition	min	typ	max	Unit
Output voltage	V_O	T_j=25˚C	8.64	9	9.36	V
Line regulation	REG_{IN}	V_I=9.5 to 15V, T_j=25˚C	—	9	100	mV
Load regulation	REG_L	I_O=1 to 40mA, T_j=25˚C	—	17	70	mV
		I_O=1 to 50mA, T_j=25˚C	—	37	75	mV
Minimum I/O voltage difference	$V_{DIF\ (min.)}$	V_I=8.8V, I_O=20mA, T_j=25˚C	—	0.07	0.2	V
		V_I=8.8V, I_O=50mA, T_j=25˚C	—	0.14	0.3	V
Bias current	I_{bias}	I_O=0mA, T_j=25˚C	—	0.8	1.4	mA
Ripple rejection ratio	RR	V_I=10 to 12V, f=120Hz	47	59	—	dB
Output noise voltage	V_{no}	f=10Hz to 100kHz	—	150	—	μV
Output voltage temperature coefficient	$\Delta V_O/Ta$	T_j=–30 to+125˚C	—	0.45	—	mV/˚C

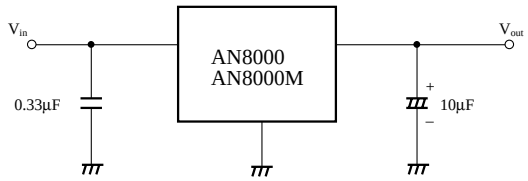
Note1) The specified condition T_j=25˚C means that the test should be conducted with each test time reduced (within 10ms) so that the drift in characteristic value due to a temperature rise at chip junction can be ignored.
Note2) Unless otherwise specified, V_I=10V, I_O=20mA, C_O=10μF

• AN8010/AN8010M (10V Type)

Parameter	Symbol	Condition	min	typ	max	Unit
Output voltage	V_O	T_j=25˚C	9.6	10	10.4	V
Line regulation	REG_{IN}	V_I=10.5 to 16V, T_j=25˚C	—	10	100	mV
Load regulation	REG_L	I_O=1 to 40mA, T_j=25˚C	—	18	75	mV
		I_O=1 to 50mA, T_j=25˚C	—	40	85	mV
Minimum I/O voltage difference	$V_{DIF\ (min.)}$	V_I=9.8V, I_O=20mA, T_j=25˚C	—	0.07	0.2	V
		V_I=9.8V, I_O=50mA, T_j=25˚C	—	0.14	0.3	V
Bias current	I_{bias}	I_O=0mA, T_j=25˚C	—	0.8	1.4	mA
Ripple rejection ratio	RR	V_I=11 to 13V, f=120Hz	46	58	—	dB
Output noise voltage	V_{no}	f=10Hz to 100kHz	—	165	—	μV
Output voltage temperature coefficient	$\Delta V_O/Ta$	T_j=–30 to+125˚C	—	0.5	—	mV/˚C

Note1) The specified condition T_j=25˚C means that the test should be conducted with each test time reduced (within 10ms) so that the drift in characteristic value due to a temperature rise at chip junction can be ignored.
Note2) Unless otherwise specified, V_I=11V, I_O=20mA, C_O=10μF

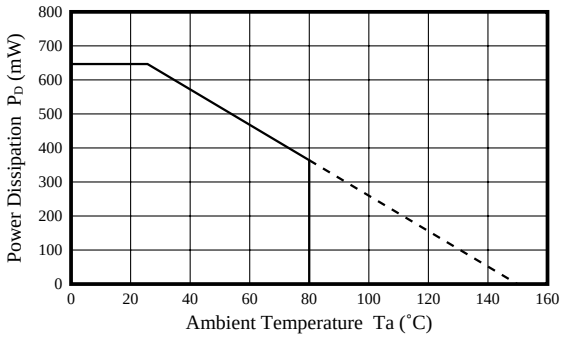
■ Application Circuit



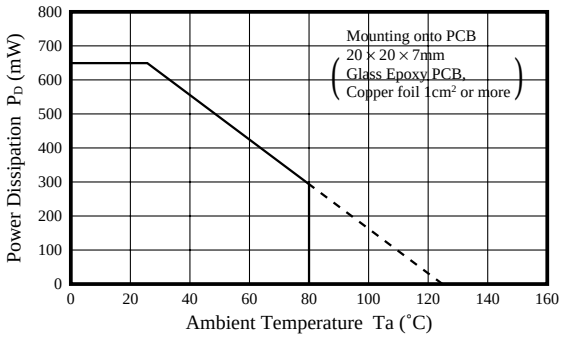
- The AN8000/AN8000M series has IC internal gain increased in order to improve performance. When the power line on the output side is long, use a capacitor of 10μF.
  For the capacitor on the output side, attach it as close to the IC as possible.
- When using at a low temperature, it is recommended to use the capacitors with low internal impedance (for example, tantalum capacitor) for output capacitors.

■ Characteristic Curve

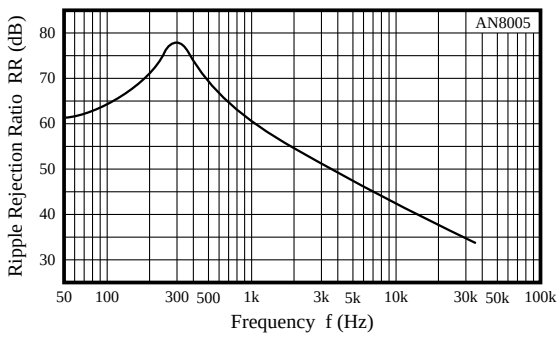
P_D–Ta (AN8000 Series)



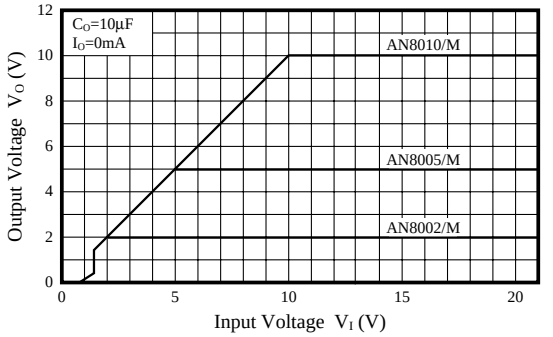
P_D–Ta (AN8000M Series)



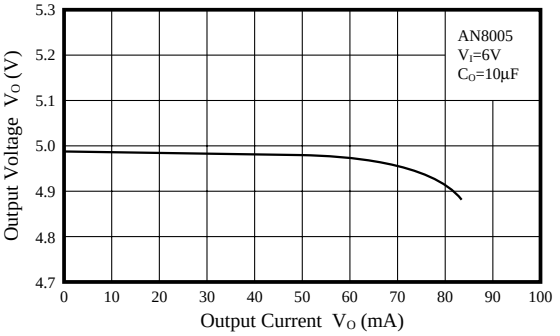
RR– f



V_O–V_I



V_O– I_O



V_O–Ta