National Semiconductor

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MM70C95/MM80C95, MM70C97/MM80C97 TRI-STATE® Hex Buffers MM70C96/MM80C96, MM70C98/MM80C98 TRI-STATE Hex Inverters

General Description

These gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. The MM70C95/MM80C95 and the MM70C97/MM80C97 convert CMOS or TTL outputs to TRI-STATE outputs with no logic inversion, the MM70C96/MM80C96 and the MM70C98/MM80C98 provide the logical opposite of the input signal. The MM70C95/MM80C95 and the MM70C96/MM80C96 have common TRI-STATE controls for all six devices. The MM70C97/MM80C97 and the MM70C98/MM80C98 have two TRI-STATE controls; one for two devices and one for the other four devices. Inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

Features

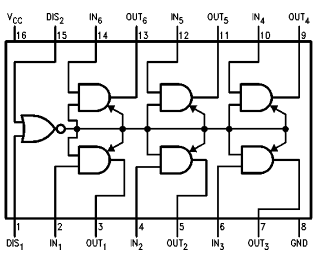
- Wide supply voltage range — 3.0V to 15V
- Guaranteed noise margin — 1.0V
- High noise immunity — 0.45 V_{CC} (typ.)
- TTL compatible — Drive 1 TTL Load

Applications

- Bus drivers — Typical propagation delay into 150 pF load is 40 ns

Connection Diagrams (Dual-In-Line Packages)

MM70C95/MM80C95

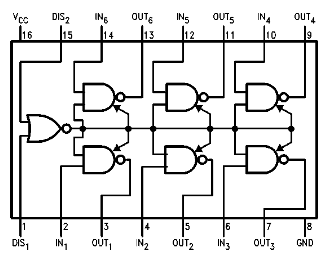


TL/F/5907–1

Top View

Order Number MM70C95 or MM80C95

MM70C96/MM80C96



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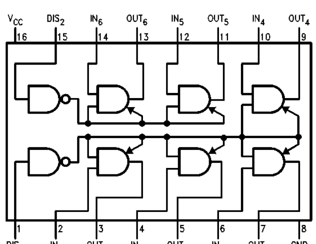
Top View

Order Number MM70C96 or MM80C96

MM70C97/MM80C97

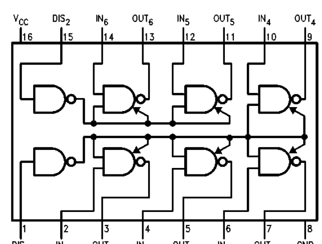


TL/F/5907–3

Top View

Order Number MM70C97 or MM80C97

MM70C98/MM80C98



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Top View

Order Number MM70C98 or MM80C98

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RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin	$-0.3V$ to $V_{CC} + 0.3V$
Operating Temperature Range	
MM70CXX	$-55°C$ to $+125°C$
MM80CXX	$-40°C$ to $+85°C$
Storage Temperature Range	$-65°C$ to $+150°C$
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Power Supply Voltage (V_{CC})	18V
Lead Temperature	
(Soldering, 10 seconds)	260°C

DC Electrical Characteristics Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current		-1.0	-0.005		μA
I_{OZ}	Output Current in High Impedance State	$V_{CC} = 15V, V_O = 15V$ $V_{CC} = 15V, V_O = 0V$	 -1.0	0.005 -0.005	1.0	μA μA
I_{CC}	Supply Current	$V_{CC} = 15V$		0.01	15	μA
TTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	70C $V_{CC} = 4.5V$ 80C $V_{CC} = 4.75V$	$V_{CC} - 1.5$ $V_{CC} - 1.5$			V V
$V_{IN(0)}$	Logical "0" Input Voltage	70C $V_{CC} = 4.5V$ 80C $V_{CC} = 4.75V$			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	70C $V_{CC} = 4.5V, I_O = -1.6$ mA 80C $V_{CC} = 4.75V, I_O = -1.6$ mA	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	70C $V_{CC} = 4.5V, I_O = 1.6$ mA 80C $V_{CC} = 4.75V, I_O = 1.6$ mA			0.4 0.4	V V
OUTPUT DRIVE (Short Circuit Current)						
I_{SOURCE}	Output Source Current	$V_{CC} = 5V, V_{IN(1)} = 5V$ $T_A = 25°C, V_{OUT} = 0V$	-4.35			mA
I_{SOURCE}	Output Source Current	$V_{CC} = 10V, V_{IN(1)} = 10V$ $T_A = 25°C, V_{OUT} = 0V$	-20			mA
I_{SINK}	Output Sink Current	$V_{CC} = 5V, V_{IN(0)} = 0V$ $T_A = 25°C, V_{OUT} = V_{CC}$	4.35			mA
I_{SINK}	Output Sink Current	$V_{CC} = 10V, V_{IN(0)} = 0V$ $T_A = 25°C, V_{OUT} = V_{CC}$	20			mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

AC Electrical Characteristics* $T_A = 25°C$, $C_L = 50$ pF, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}, t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from Data Input to Output					
	MM70C95/MM80C95, MM70C97/MM80C97	$V_{CC} = 5V$		60	100	ns
		$V_{CC} = 10V$		25	40	ns
	MM70C96/MM80C96, MM70C98/MM80C98	$V_{CC} = 5V$		70	150	ns
		$V_{CC} = 10V$		35	75	ns
t_{pd0}, t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from Data Input to Output					
	MM70C95/MM80C95, MM70C97/MM80C97	$V_{CC} = 5V$, $C_L = 150$ pF		85	160	ns
		$V_{CC} = 10V$, $C_L = 150$ pF		40	80	ns
	MM70C96/MM80C96, MM70C98/MM80C98	$V_{CC} = 5V$, $C_L = 150$ pF		95	210	ns
		$V_{CC} = 10V$, $C_L = 150$ pF		45	110	ns
t_{1H}, t_{0H}	Delay from Disable Input to High Impedance State, (from Logical "1" or Logical "0")	$R_L = 10k$, $C_L = 5$ pF				
	MM70C95/MM80C95	$V_{CC} = 5V$		80	135	ns
		$V_{CC} = 10V$		50	90	ns
	MM70C96/MM80C96	$V_{CC} = 5V$		100	180	ns
		$V_{CC} = 10V$		70	125	ns
	MM70C97/MM80C97	$V_{CC} = 5V$		70	125	ns
		$V_{CC} = 10V$		50	90	ns
	MM70C98/MM80C98	$V_{CC} = 5V$		90	170	ns
		$V_{CC} = 10V$		70	125	ns
t_{H1}, t_{H0}	Delay from Disable Input to Logical "1" Level (from High Impedance State)	$R_L = 10k$, $C_L = 50$ pF				
	MM70C95/MM80C95	$V_{CC} = 5V$		120	200	ns
		$V_{CC} = 10V$		50	90	ns
	MM70C96/MM80C96	$V_{CC} = 5V$		130	225	ns
		$V_{CC} = 10V$		60	110	ns
	MM70C97/MM80C97	$V_{CC} = 5V$		95	175	ns
		$V_{CC} = 10V$		40	80	ns
	MM70C98/MM80C98	$V_{CC} = 5V$		120	200	ns
		$V_{CC} = 10V$		50	90	ns
C_{IN}	Input Capacitance	Any Input (Note 2)		5.0		pF
C_{OUT}	Output Capacitance TRI-STATE	Any Output (Note 2)		11		pF
C_{PD}	Power Dissipation Capacitance	(Note 3)		60		pF

*AC Parameters are guaranteed by DC correlated testing.

Truth Tables

MM70C95/MM80C95

Disable DIS_1	Input DIS_2	Input	Output
0	0	0	0
0	0	1	1
0	1	X	H-z
1	0	X	H-z
1	1	X	H-z

MM70C96/MM80C96

Disable DIS_1	Input DIS_2	Input	Output
0	0	0	1
0	0	1	0
0	1	X	H-z
1	0	X	H-z
1	1	X	H-z

MM70C97/MM80C97

Disable DIS_4	Input DIS_2	Input	Output
0	0	0	0
0	0	1	1
X	1	X	H-z*
1	X	X	H-z**

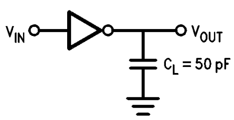
MM70C98/MM80C98

Disable DIS_4	Input DIS_2	Input	Output
0	0	0	1
0	0	1	0
X	1	X	H-z*
1	X	X	H-z**

*Output 5–6 only
**Output 1–4 only
X = Irrelevant

AC Test Circuits and Switching Time Waveforms

t_{pd0}, t_{pd1}



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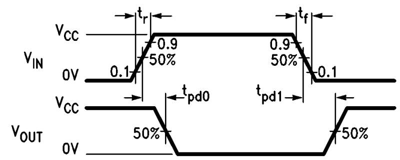
CMOS to CMOS



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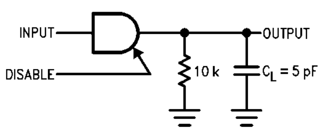
t_{1H} and t_{H1}



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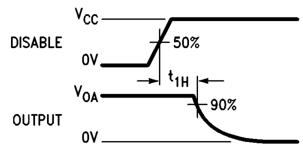
t_{1H}



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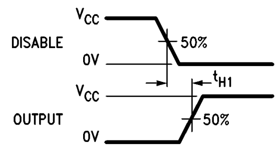
t_{H1}



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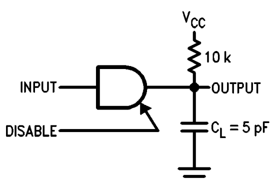
t_{0H} and t_{H0}



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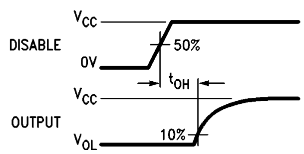
t_{0H}



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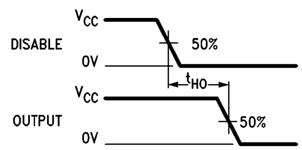
t_{H0}



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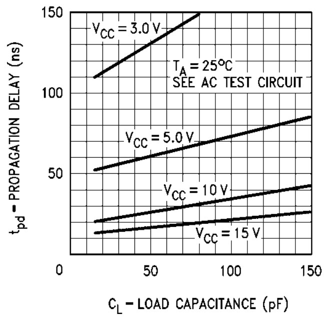
Note: Delays measured with input t_r, $t_f \leq 20$ ns.

Typical Performance Characteristics

Propagation Delay vs Load Capacitance



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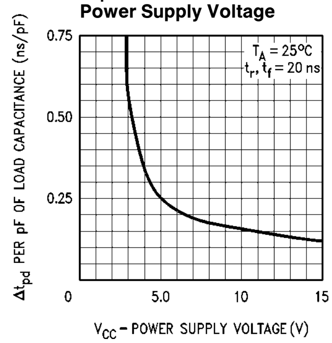
Δt_{pd}/pF vs Power Supply Voltage



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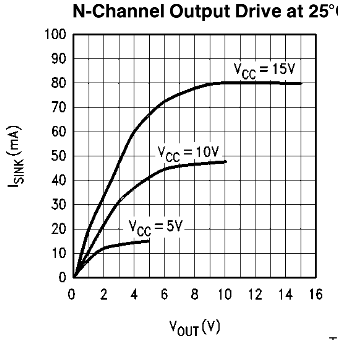
N-Channel Output Drive at 25°C



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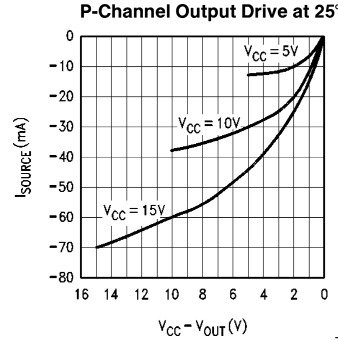
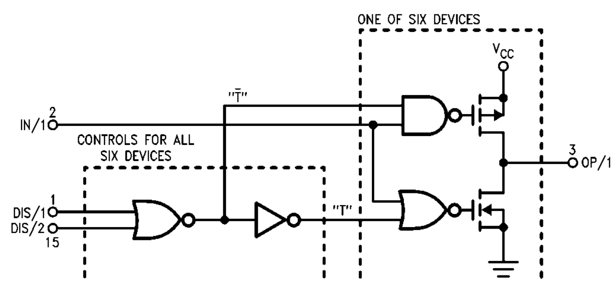
P-Channel Output Drive at 25°C



TL/F/5907–8

Schematic Diagrams

MM70C95/MM80C95 TRI-STATE



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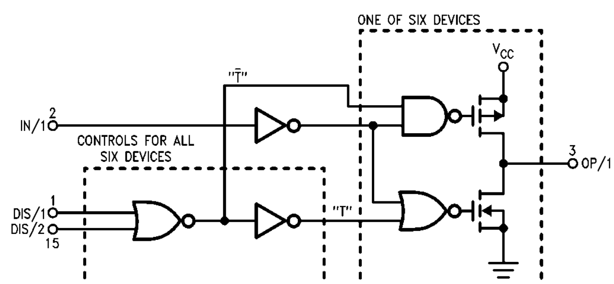
MM70C96/MM80C96 TRI-STATE



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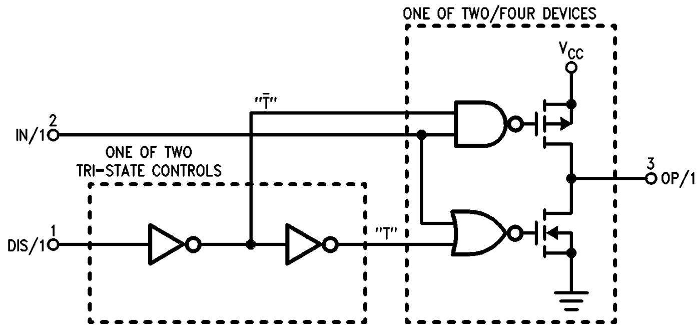
Schematic Diagrams (Continued)

MM70C97/MM80C97 TRI-STATE



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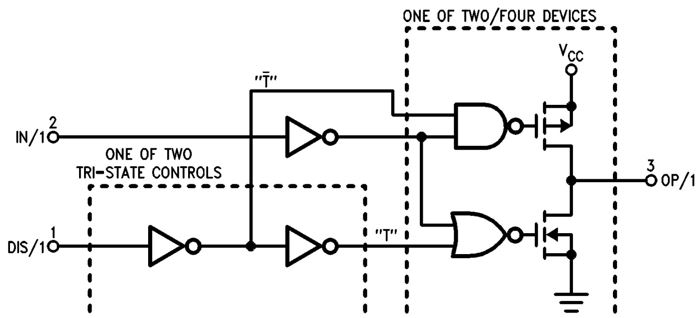
MM70C98/MM80C98 TRI-STATE



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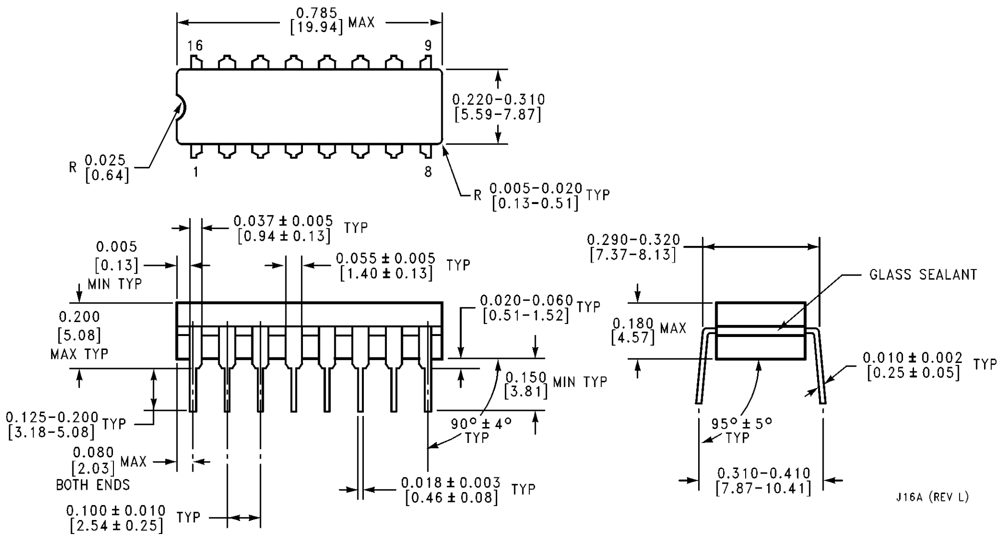
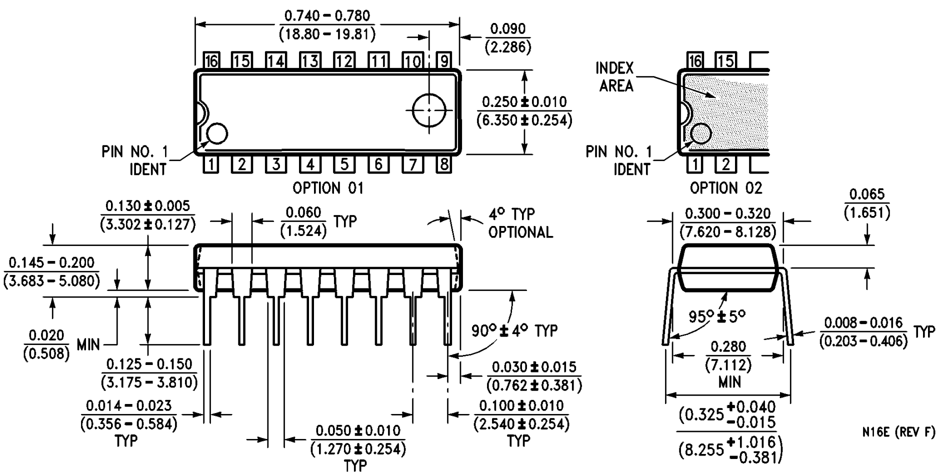
Physical Dimensions inches (millimeters)



Ceramic Dual-In-Line Package (J)
Order Number MM70C95J, MM70C96J, MM70C97J, MM70C98J, MM80C95J, MM80C96J, MM80C97J or MM80C98J
NS Package Number J16A

Physical Dimensions inches (millimeters) (Continued)



Molded Dual-In-Line Package (N)
Order Number MM70C95N, MM70C96N, MM70C97N, MM70C98N, MM80C95N, MM80C96N, MM80C97N or MM80C98N
NS Package Number N16E

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National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408