National Semiconductor

February 1988

MM54C941/MM74C941 Octal Buffers/Line Receivers/ Line Drivers with TRI-STATE® Outputs

General Description

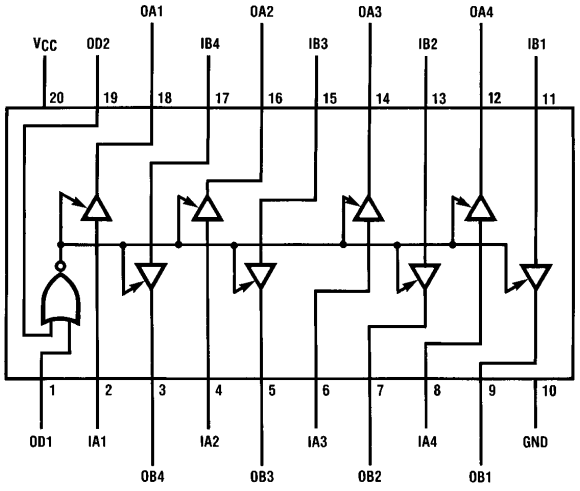
These octal buffers and line drivers are monolithic complementary MOS (CMOS) integrated circuits with TRI-STATE outputs. These outputs have been specially designed to drive highly capacitive loads such as bus-oriented systems. These devices have a fan-out of 6 low power Schottky loads. When V_{CC} = 5V, inputs can accept true TTL high and low logic levels.

Features

- Wide supply voltage range (3V to 15V)
- Low power consumption
- TTL compatibility (Improved on the inputs)
- High capacitive load
- TRI-STATE outputs
- Input protection
- 20-pin dual-in-line package
- High output drive

Connection and Logic Diagrams

Dual-In-Line Package



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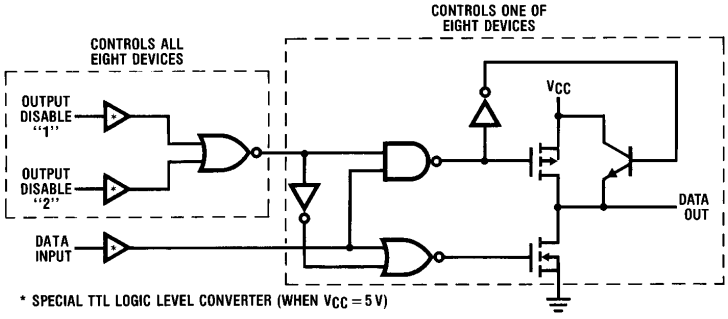
Top View

Order Number MM54C941 or MM74C941



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RRD-B30M105/Printed in U. S. A.

MM54C941/MM74C941 Octal Buffers/Line Receivers/Line Drivers with TRI-STATE Outputs

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin	0.3V to V_{CC} + 0.3V
Operating Temperature Range (T_A)	
MM54C941	−55°C to +125°C
MM74C941	−40°C to +85°C
Storage Temperature Range (T_S)	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{CC} Range	3V to 15V
V_{CC}	18V
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

DC Electrical Characteristics Min/Max limits apply across temperature range, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5.0V V_{CC} = 10V	2.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5.0V V_{CC} = 10V			0.8 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5.0V, I_O = −10μA V_{CC} = 10V, I_O = −10μA	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5.0V, I_O = 10 μA V_{CC} = 10V, I_O = 10 μA			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
I_{CC}	Supply Current	V_{CC} = 15V		0.05	300	μA
I_{OZ}	TRI-STATE Leakage	V_{CC} = 15V, V_{OUT} = 0V or 15V			±10	μA
CMOS/TTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V	V_{CC}−2.5 V_{CC}−2.5			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, V_{CC} = 4.5V, I_O = −450 μA 74C, V_{CC} = 4.75V, I_O = −450 μA 54C, V_{CC} = 4.5V, I_O = −2.2 mA 74C, V_{CC} = 4.75V, I_O = −2.2 mA	V_{CC}−0.4 V_{CC}−0.4 2.4 2.4			V V V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, V_{CC} = 4.5V, I_O = 2.2 mA 74C, V_{CC} = 4.75V, I_O = 2.2 mA			0.4 0.4	V V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)						
I_{SOURCE}	Output Source Current (P-Channel)	V_{CC} = 5.0V, V_{OUT} = 0V T_A = 25°C	−14.0	−30.0		mA
I_{SOURCE}	Output Source Current (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V T_A = 25°C	−36.0	−70.0		mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC} T_A = 25°C	12.0	20.0		mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC} T_A = 25°C	48.0	70		mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

AC Electrical Characteristics* $T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd1}, t_{pd0}	Propagation Delay (Data IN to OUT)	$V_{CC} = 5.0V$, $C_L = 50$ pF		70	140	ns
		$V_{CC} = 10V$, $C_L = 50$ pF		35	70	ns
		$V_{CC} = 5.0V$, $C_L = 150$ pF		90	160	ns
		$V_{CC} = 10V$, $C_L = 150$ pF		45	90	ns
t_{IH}, t_{OH}	Propagation Delay Output Disable to Logic Level (from High Impedance State) (from a Logic Level)	$R_L = 1\ k\Omega$, $C_L = 50$ pF				
		$V_{CC} = 5.0V$		100	200	ns
		$V_{CC} = 210V$		55	110	ns
t_{H1},t_{H0}	Propagation Delay Output Disable to Logic Level (from High Impedance State)	$R_L = 1\ k\Omega$, $C_L = 50$ pF				
		$V_{CC} = 5.0V$		100	200	ns
		$V_{CC} = 10V$		55	110	ns
t_{THL}, t_{TLH}	Transition Time	$V_{CC} = 5.0V$, $C_L = 50$ pF		50	100	ns
		$V_{CC} = 10V$, $C_L = 50$ pF		30	60	ns
		$V_{CC} = 5.0V$, $C_L = 150$ pF		80	160	ns
		$V_{CC} = 10V$, $C_L = 150$ pF		50	100	ns
C_{PD}	Power Dissipation Capacitance (Output Enabled per Buffer)	(Note 3)		100		pF
	(Output Disabled per Buffer)			10		pF
C_{IN}	Input Capacitance (Any Input)	(Note 2) $V_{IN} = 0V$, f = 1 MHz, $T_A = 25°C$		10		pF
C_O	(Output Capacitance) (Output Disabled)	$V_{IN} = 0V$, f = 1 MHz, $T_A = 25°C$		10		pF

*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics Application Note, AN-90.

Truth Table

OD1	OD2	Input	Output
0	0	0	0
0	0	1	1
0	1	X	Z
1	0	X	Z
1	1	X	Z

1 = High

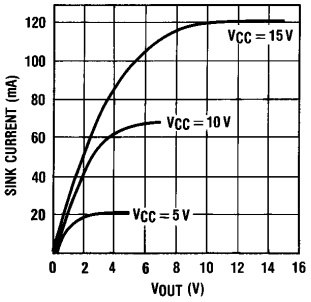
0 = Low

X = Don't Care

Z = TRI-STATE

Typical Performance Characteristics

N-Channel Output Drive @ 25°C



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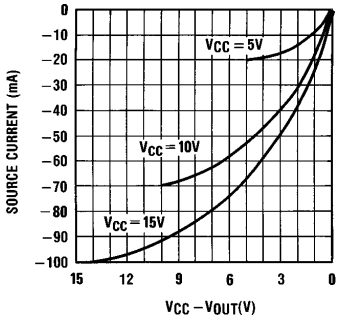
P-Channel Output Drive @ 25°C



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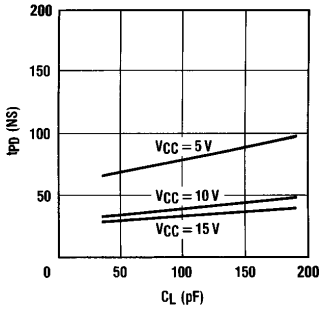
Propagation Delay vs Load Capacitance



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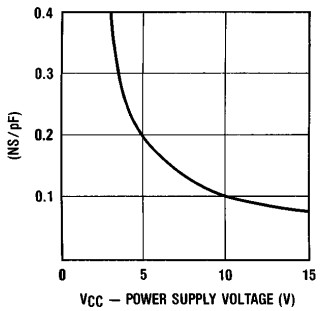
Δt_{PD} per pF of Load Capacitance



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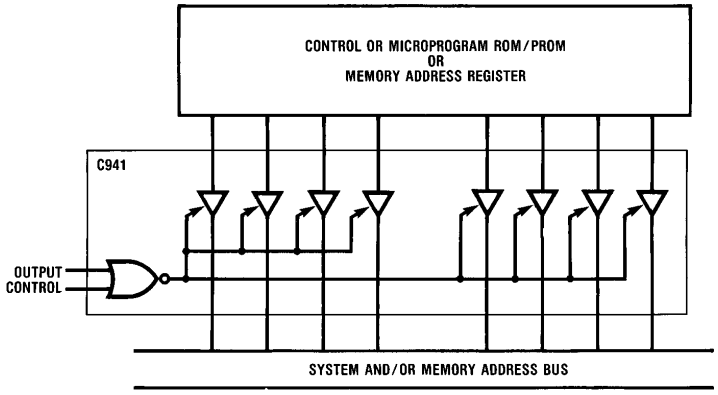
Typical Application



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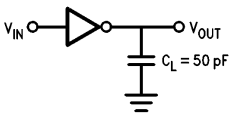
AC Test Circuits and Switching Time Waveforms

t_{pd0}, t_{pd1}



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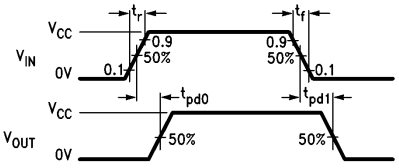
CMOS to CMOS



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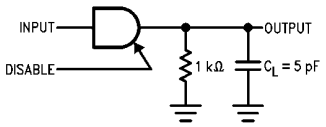
t_{1H} and t_{H1}



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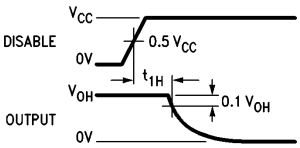
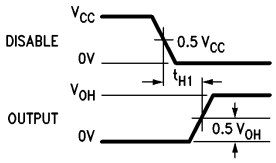
t_{1H}



t_{H1}



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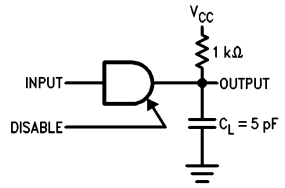
Note: V_{OH} is defined as the DC output high voltage when the device is loaded with a 1 kΩ resistor to ground.

t_{0H} and t_{H0}



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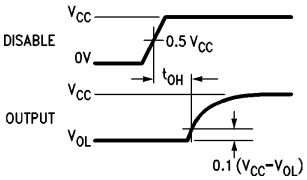
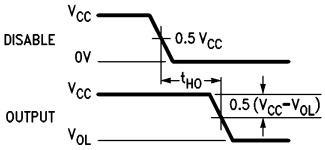
Note: Delays measured with input t_r, $t_f \leq$ 20 ns.

t_{0H}



t_{H0}



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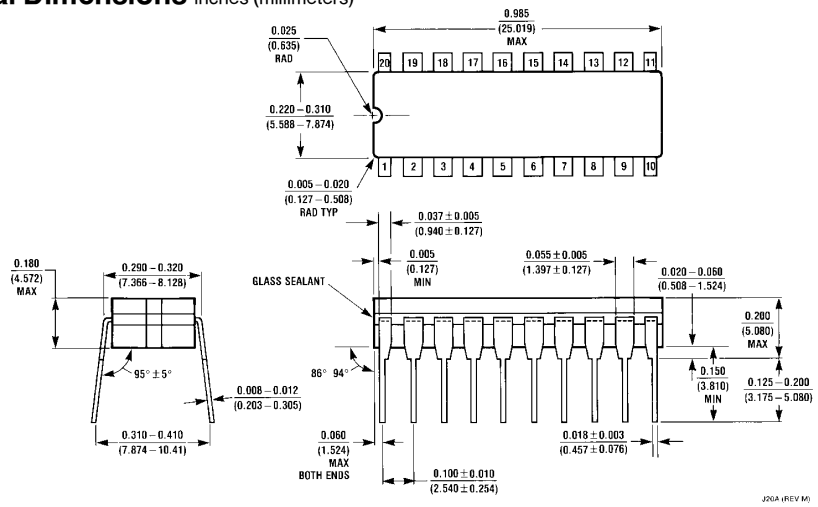
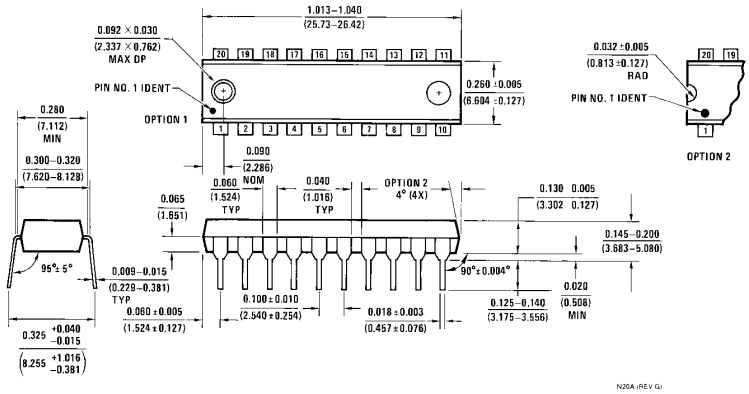
Note: V_{OL} is defined as the DC output low voltage when the device is loaded with a 1 kΩ resistor to V_{CC}.

Physical Dimensions inches (millimeters)



Ceramic Dual-In-Line Package (J)
Order Number MM54C941J or MM74C941J
NS Package Number J20A



Molded Dual-In-Line Package (N)
Order Number MM54C941N or MM74C941N
NS Package Number N20A

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