FAIRCHILD SEMICONDUCTOR™

October 1987
Revised January 1999

# MM74C89
# 64-Bit 3-STATE Random Access Read/Write Memory

## General Description

The MM74C89 is a 16-word by 4-bit random access read/write memory. Inputs to the memory consist of four address lines, four data input lines, a write enable line and a memory enable line. The four binary address inputs are decoded internally to select each of the 16 possible word locations. An internal address register latches the address information on the positive to negative transition of the memory enable input. The four 3-STATE data output lines working in conjunction with the memory enable input provide for easy memory expansion.

**Address Operation:** Address inputs must be stable $t_{SA}$ prior to the positive to negative transition of memory enable. It is thus not necessary to hold address information stable for more than $t_{HA}$ after the memory is enabled (positive to negative transition of memory enable).

**Write Operation:** Information present at the data inputs is written into the memory at the selected address by bringing write enable and memory enable LOW.

**Read Operation:** The complement of the information which was written into the memory is non-destructively read out at the four outputs. This is accomplished by selecting the desired address and bringing memory enable LOW and write enable HIGH.

When the device is writing or disabled the output assumes a 3-STATE (Hi-z) condition.

## Features

- Wide supply voltage range: 3.0V to 15V
- Guaranteed noise margin: 1.0V
- High noise immunity: 0.45 $V_{CC}$ (typ.)
- Low power TTL compatibility:
  fan out of 2 driving 74L
- Low power consumption: 100 nW/package (typ.)
- Fast access time: 130 ns (typ.) at $V_{CC}$ = 10V
- 3-STATE output

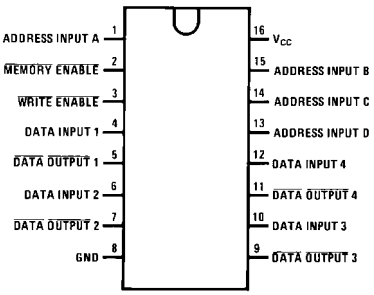
**Note:** The timing is different than the DM7489 in that a positive to negative transition of the memory enable must occur for the memory to be selected.

## Ordering Code:

| Order Number | Package Number | Package Description |
|---|---|---|
| MM74C89N | N16E | 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

## Connection Diagram

**Pin Assignments for DIP**



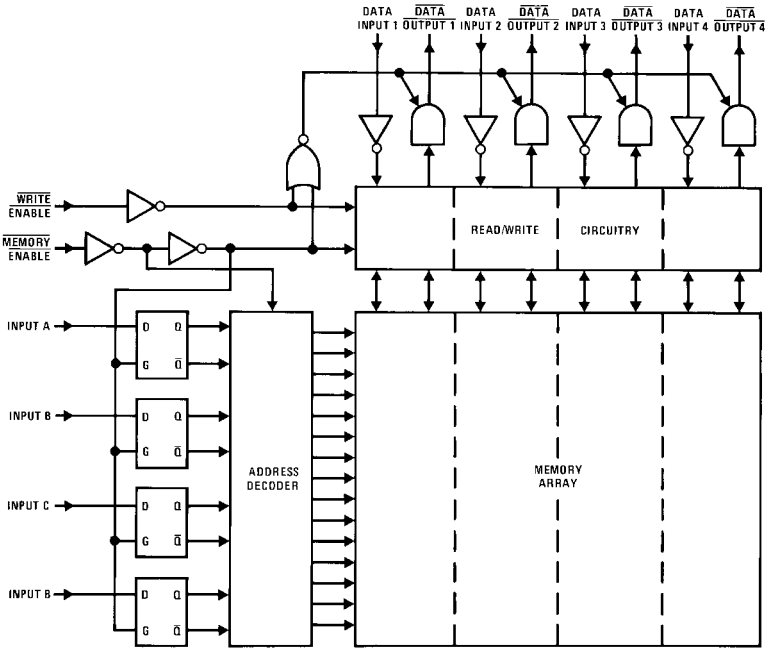

**Top View**

## Truth Table

| ME | WE | Operation | Condition of Outputs |
|---|---|---|---|
| L | L | Write | 3-STATE |
| L | H | Read | Complement of Selected Word |
| H | L | Inhibit, Storage | 3-STATE |
| H | H | Inhibit, Storage | 3-STATE |

## Logic Diagram



## Absolute Maximum Ratings (Note 1)

| | |
|---|---|
| Voltage at any Pin | −0.3V to $V_{CC}$ +0.3V |
| Operating Temperature Range | −40°C to +85°C |
| Storage Temperature Range ($T_S$) | −65°C to +150°C |
| Power Dissipation ($P_D$) | |
| Dual-In-Line | 700 mW |
| Small Outline | 500 mW |
| Operating $V_{CC}$ Range | 3.0V to 15V |
| Absolute Maximum $V_{CC}$ | 18V |
| Lead Temperature ($T_L$) | |
| (Soldering, 10 seconds) | 260°C |

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

## DC Electrical Characteristics

Min/Max limits apply across temperature range, unless otherwise noted

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **CMOS TO CMOS** | | | | | | |
| $V_{IN(1)}$ | Logical "1" Input Voltage | $V_{CC}$ = 5.0V | 3.5 | | | V |
| | | $V_{CC}$ = 10V | 8.0 | | | V |
| $V_{IN(0)}$ | Logical "0" Input Voltage | $V_{CC}$ = 5.0V | | | 1.5 | V |
| | | $V_{CC}$ = 10V | | | 2.0 | V |
| $V_{OUT(1)}$ | Logical "1" Output Voltage | $V_{CC}$ = 5.0V, $I_O$ = −10 μA | 4.5 | | | V |
| | | $V_{CC}$ = 10V, $I_O$ = −10 μA | 9.0 | | | V |
| $V_{OUT(0)}$ | Logical "0" Output Voltage | $V_{CC}$ = 5.0V, $I_O$ = +10 μA | | | 0.5 | V |
| | | $V_{CC}$ = 10V, $I_O$ = +10 μA | | | 1.0 | V |
| $I_{IN(1)}$ | Logical "1" Input Current | $V_{CC}$ = 15V, $V_{IN}$ = 15V | | −0.005 | 1.0 | μA |
| $I_{IN(0)}$ | Logical "0" Input Current | $V_{CC}$ = 15V, $V_{IN}$ = 0V | −1.0 | −0.005 | | μA |
| $I_{OZ}$ | Output Current in High | $V_{CC}$ = 15V, V = 15V | | 0.005 | 1.0 | μA |
| | Impedance State | $V_{CC}$ = 15V, $V_O$ = 0V | −1.0 | −0.005 | | μA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = 15V | | 0.05 | 300 | μA |
| **CMOS/LPTTL INTERFACE** | | | | | | |
| $V_{IN(1)}$ | Logical "1" Input Voltage | $V_{CC}$ = 4.75V | $V_{CC}$ − 1.5 | | | V |
| $V_{IN(0)}$ | Logical "0" Input Voltage | $V_{CC}$ = 4.75V | | | 0.8 | V |
| $V_{OUT(1)}$ | Logical "1" Output Voltage | $V_{CC}$ = 4.75V, $I_O$ = −360 μA | 2.4 | | | V |
| $V_{OUT(0)}$ | Logical "0" Output Voltage | $V_{CC}$ = 4.75V, $I_O$ = +360 μA | | | 0.4 | V |
| **OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)** | | | | | | |
| $I_{SOURCE}$ | Output Source Current | $V_{CC}$ = 5.0V, $V_{OUT}$ = 0V | −1.75 | −3.3 | | mA |
| | (P-Channel) | $T_A$ = 25°C | | | | |
| $I_{SOURCE}$ | Output Source Current | $V_{CC}$ = 10V, $V_{OUT}$ = 0V | −8.0 | −15 | | mA |
| | (P-Channel) | $T_A$ = 25°C | | | | |
| $I_{SINK}$ | Output Sink Current | $V_{CC}$ = 5.0V, $V_{OUT}$ = $V_{CC}$ | 1.75 | 3.6 | | mA |
| | (N-Channel) | $T_A$ = 25°C | | | | |
| $I_{SINK}$ | Output Sink Current | $V_{CC}$ = 10V, $V_{OUT}$ = $V_{CC}$ | 8.0 | 16 | | mA |
| | (N-Channel) | $T_A$ = 25°C | | | | |

## AC Electrical Characteristics (Note 2)

$T_A = 25°C$, $C_L = 50$ pF, unless otherwise noted

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $t_{pd}$ | Propagation Delay from | $V_{CC} = 5V$ | | 270 | 500 | ns |
| | Memory Enable | $V_{CC} = 10V$ | | 100 | 220 | ns |
| $t_{ACC}$ | Access Time from | $V_{CC} = 5V$ | | 350 | 650 | ns |
| | Address Input | $V_{CC} = 10V$ | | 130 | 280 | ns |
| $t_{SA}$ | Address Setup Time | $V_{CC} = 5V$ | 150 | | | ns |
| | | $V_{CC} = 10V$ | 60 | | | ns |
| $t_{HA}$ | Address Hold Time | $V_{CC} = 5V$ | 60 | | | ns |
| | | $V_{CC} = 10V$ | 40 | | | ns |
| $t_{ME}$ | Memory Enable Pulse Width | $V_{CC} = 5V$ | 400 | 250 | | ns |
| | | $V_{CC} = 10V$ | 150 | 90 | | ns |
| $t_{SR}$ | Write Enable Setup | $V_{CC} = 5V$ | 0 | | | ns |
| | Time for a Read | $V_{CC} = 10V$ | 0 | | | ns |
| $t_{WS}$ | Write Enable Setup | $V_{CC} = 5V$ | | | $t_{ME}$ | ns |
| | Time for a Write | $V_{CC} = 10V$ | | | $t_{ME}$ | ns |
| $t_{WE}$ | Write Enable Pulse Width | $V_{CC} = 5V$, $t_{WS} = 0$ | 300 | 160 | | ns |
| | | $V_{CC} = 10V$, $t_{WS} = 0$ | 100 | 60 | | ns |
| $t_{HD}$ | Data Input Hold Time | $V_{CC} = 5V$ | 50 | | | ns |
| | | $V_{CC} = 10V$ | 25 | | | ns |
| $t_{SD}$ | Data Input Setup | $V_{CC} = 5V$ | 50 | | | ns |
| | | $V_{CC} = 10V$ | 25 | | | ns |
| $t_{1H}$, $t_{0H}$ | Propagation Delay from a Logical | $V_{CC} = 5V$, $C_L = 5$ pF, $R_L = 10k$ | | 180 | 300 | ns |
| | "1" or Logical "0" to the High | $V_{CC} = 10V$, $C_L = 5$ pF, $R_L = 10k$ | | −85 | 120 | ns |
| | Impedance State from | | | | | |
| | Memory Enable | | | | | |
| $t_{1H}$, $t_{0H}$ | Propagation Delay from a Logical | $V_{CC} = 50V$, $C_L = 5$ pF, $R_L = 10k$ | | 180 | 300 | ns |
| | "1" or Logical "0" to the High | $V_{CC} = 10V$, $C_L = 5$ pF, $R_L = 10k$ | | 85 | 120 | ns |
| | Impedance State from | | | | | |
| | Write Enable | | | | | |
| $C_{IN}$ | Input Capacity | Any Input (Note 3) | | 5 | | pF |
| $C_{OUT}$ | Output Capacity | Any Output (Note 3) | | 6.5 | | pF |
| $C_{PD}$ | Power Dissipation Capacity | (Note 4) | | 230 | | pF |

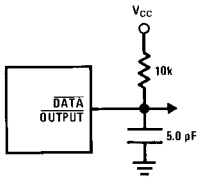
**Note 2:** AC Parameters are guaranteed by DC correlated testing.

**Note 3:** Capacitance is guaranteed by periodic testing.

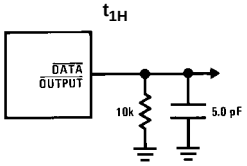
**Note 4:** $C_{PD}$ determines the no load AC power consumption of any CMOS device. For complete explanation see Family Characteristics application note, AN-90.

## AC Test Circuits

$t_{0H}$

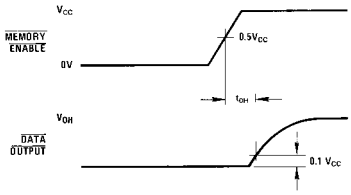



$t_{1H}$

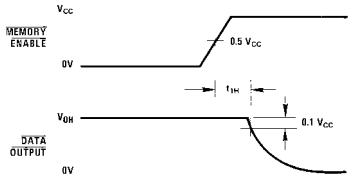



## Switching Time Waveforms

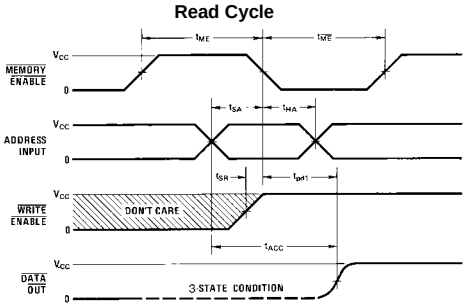
$t_{0H}$



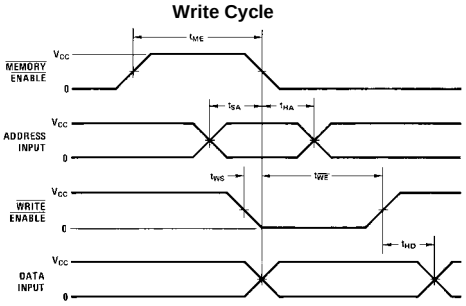

$t_{1H}$



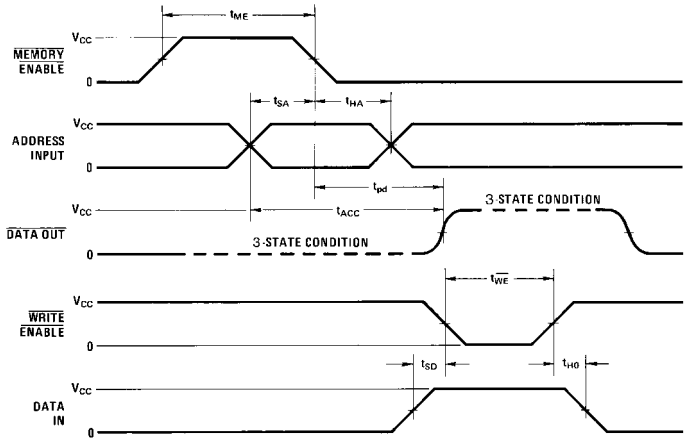

**Read Cycle**




**Write Cycle**



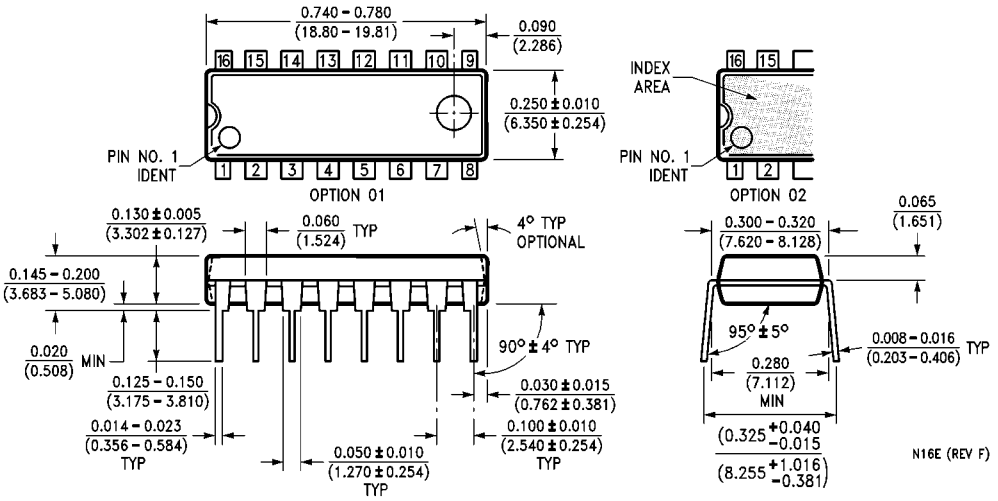

**Read Modify Write Cycle**




$t_f$ = 10 ns

$t_r$ = 60 ns

## Physical Dimensions inches (millimeters) unless otherwise noted




**16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide**
**Package Number N16E**

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