5 MHz Single-Supply Operational Amplifiers

OP183/OP283

FEATURES

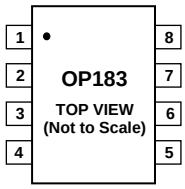
Single-Supply – +3 Volts to +36 Volts
Wide Bandwidth – 5 MHz
Low Offset Voltage – <1 mV
High Slew Rate – 10 V/μs
Low Noise – 10 nV/√Hz
Unity-Gain Stable
Input and Output Range Includes GND
No Phase Reversal

APPLICATIONS

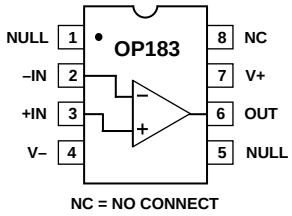
Multimedia
Telecom
ADC Buffers
Wide Band Filters
Microphone Preamplifiers

PIN CONNECTIONS

8-Lead Narrow-Body SO (S Suffix)

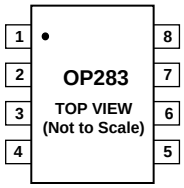


8-Lead Epoxy DIP (P Suffix)

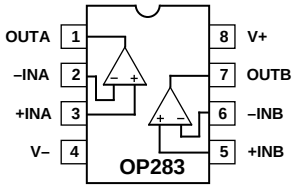


NC = NO CONNECT

8-Lead Narrow-Body SO (S Suffix)



8-Lead Epoxy DIP (P Suffix)



GENERAL DESCRIPTION

The OP183 is a single-supply, 5 MHz bandwidth amplifier with slew rates of 10 V/μs. The OP283 is a dual version. Both can operate from voltages as low as 3 volts and up to 36 volts. This combination of slew rate and bandwidth yields excellent single-supply ac performance making them ideally suited for telecom and multimedia audio applications.

In addition to its ac characteristics, the OP183 family provides good dc performance with guaranteed 1 mV offset. Noise is a respectable 10 nV/√Hz. Supply current is only 1.2 mA per amplifier.

These amplifiers are well suited for single-supply applications that require moderate bandwidths even when used in high gain configurations. This makes them useful in filters and instrumentation. Their output drive capability and very wide full power bandwidth make them a good choice for multimedia headphone drivers or microphone input amplifiers.

The OP183 and OP283 are available in 8-pin plastic DIP and SO-8 surface mount packages. They are specified over the extended industrial (–40°C to +85°C) temperature range.

REV. B

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OP183/OP283–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = +5.0 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	V_{CM} = 2.5 V, V_{OUT} = 2.5 V,		0.025	1.0	mV
		–40°C ≤ T_A ≤ +85°C			1.25	mV
Input Bias Current	I_B	V_{CM} = 2.5 V, V_{OUT} = 2.5 V,		350	600	nA
		–40°C ≤ T_A ≤ +85°C		430	750	nA
Input Offset Current	I_{OS}	V_{CM} = 2.5 V, V_{OUT} = 2.5 V,				nA
		–40°C ≤ T_A ≤ +85°C		11	±50	nA
Input Voltage Range			0		+3.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 to 3.5 V				
		–40°C ≤ T_A ≤ +85°C	70	104		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, 0.2 ≤ V_O ≤ 3.8 V	100			V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			4		µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			–1.6		nA/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 2 kΩ to GND	+4.0	4.22		V
Output Voltage Low	V_{OL}	R_L = 2 kΩ to GND		50	75	mV
Short Circuit Limit	I_{SC}	Source		25		mA
		Sink		30		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = +4 V to +6 V,				
		–40°C ≤ T_A ≤ +85°C	70	104		dB
Supply Current/Amplifier	I_{SY}	V_O = 2.5 V,				
		–40°C ≤ T_A ≤ +85°C		1.2	1.5	mA
Supply Voltage Range	V_S		+3		±18	V
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ	5	10		V/µs
Full-Power Bandwidth	BWp	1% Distortion		>50		kHz
Settling Time	t_S	To 0.01%		1.5		µs
Gain Bandwidth Product	GBP			5		MHz
Phase Margin	ϕm			46		Degrees
NOISE PERFORMANCE						
Voltage Noise	$e_{n\ p\text{-}p}$	0.1 Hz to 10 Hz		2		µV p-p
Voltage Noise Density	e_n	f = 1 kHz, V_{CM} = 2.5 V		10		nV/√Hz
Current Noise Density	i_n			0.4		pA/√Hz

ELECTRICAL CHARACTERISTICS (@ V_S = +3.0 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	V_{CM} = 1.5 V, V_{OUT} = 1.5 V,		0.3	1.0	mV
		–40°C ≤ T_A ≤ +85°C			1.25	mV
Input Bias Current	I_B	V_{CM} = 1.5 V, V_{OUT} = 1.5 V,		350	600	nA
		–40°C ≤ T_A ≤ +85°C			750	nA
Input Offset Current	I_{OS}	V_{CM} = 1.5 V, V_{OUT} = 1.5 V,				nA
		–40°C ≤ T_A ≤ +85°C		11	±50	nA
Input Voltage Range			0		+1.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 1.5 V,				
		–40°C ≤ T_A ≤ +85°C	70	103		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, 0.2 ≤ V_O ≤ 1.8 V	100	260		V/mV
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 2 kΩ to GND	+2.0	2.25		V
Output Voltage Low	V_{OL}	R_L = 2 kΩ to GND		90	125	mV
Short Circuit Limit	I_{SC}	Source		25		mA
		Sink		30		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = +2.5 V to +3.5 V,				
		–40°C ≤ T_A ≤ +85°C	60	113		dB
Supply Current/Amplifier	I_{SY}	–40°C ≤ T_A ≤ +85°C, V_O = 1.5 V		1.2	1.5	mA
DYNAMIC PERFORMANCE						
Gain Bandwidth Product	GBP			5		MHz
NOISE PERFORMANCE						
Voltage Noise Density	e_n	f = 1 kHz, V_{CM} = 1.5 V		10		nV/√Hz

ELECTRICAL CHARACTERISTICS (@ V_S = ±15.0 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			0.01	1.0	mV
		–40°C ≤ T_A ≤ +85°C			1.25	mV
Input Bias Current	I_B			300	600	nA
		–40°C ≤ T_A ≤ +85°C		400	750	nA
Input Offset Current	I_{OS}	–40 ≤ T_A ≤ +85°C		11	±50	nA
Input Voltage Range			–15		+13.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = –15 V to +13.5 V,				
		–40°C ≤ T_A ≤ +85°C	70	86		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ	100	1000		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			3		µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			–1.6		nA/°C
Long Term Offset Voltage	V_{OS}	Note 1			1.5	mV
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 2 kΩ to GND, –40°C ≤ T_A ≤ +85°C	+13.9	14.1		V
Output Voltage Low	V_{OL}	R_L = 2 kΩ to GND, –40°C ≤ T_A ≤ +85°C		–14.05	–13.9	V
Short-Circuit Limit	I_{SC}	Source		30		mA
		Sink		50		mA
Open -Loop Output Impedance	Z_{OUT}	f = 1 MHz, A_V = +1		15		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±2.5 V to ±18 V,				
		–40°C ≤ T_A ≤ +85°C	70	112		dB
Supply Current/Amplifier	I_{SY}	V_S = ±18 V, V_O = 0 V,				
		–40°C ≤ T_A ≤ +85°C		1.2	1.75	mA
Supply Voltage Range	V_S		+3		±18	V
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ	10	15		V/µs
Full-Power Bandwidth	BW_p	1% Distortion		50		kHz
Settling Time	t_S	To 0.01%		1.5		µs
Gain Bandwidth Product	GBP			5		MHz
Phase Margin	ϕm			56		degrees
NOISE PERFORMANCE						
Voltage Noise	$e_{n\ p\text{-}p}$	0.1 Hz to 10 Hz		2		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		10		nV/√Hz
Current Noise Density	i_n			0.4		pA/√Hz

NOTES
[1]Long term offset voltage is guaranteed by a 1000 hour life test performed on three independent lots at +125 °C, with an LTPD of 1.3.

Specifications subject to change without notice.

WAFER TEST LIMITS (@ V_S = +5.0 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Limit	Units
Offset Voltage	V_{OS}	V_S = ±15 V, V_O = 0 V	1.0	mV max
Input Bias Current	I_B	V_{CM} = 2.5 V	±600	nA max
Input Offset Current	I_{OS}	V_{CM} = 2.5 V	±50	nA max
Common-Mode Rejection	CMRR	V_{CM} = 0 V to 3.5 V	70	dB min
Power Supply Rejection Ratio	PSRR	V = ±2.5 V to ±18 V	70	dB min
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, 0.2 ≤ V_O ≤ 3.8 V	100	V/mV min
Output Voltage High	V_{OH}	R_L = 2 kΩ	4.0	V min
Output Voltage Low	V_{OL}	R_L = 2 kΩ	75	mV max
Supply Current/Amplifier	I_{SY}	V_S = ±15 V, V_O = 0 V, R_L = ∞	1.5	mA max

NOTE
Electrical tests and wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage ..... ±18 V
Input Voltage ..... ±18 V
Differential Input Voltage[2] ..... ±7 V
Output Short-Circuit Duration to GND ..... Indefinite
Storage Temperature Range
P, S Package ..... –65°C to +150°C
Operating Temperature Range
OP183/OP283G ..... –40°C to +85°C
Junction Temperature Range
P, S Package .....–65°C to +150°C
Lead Temperature Range (Soldering 60 Sec) ..... +300°C

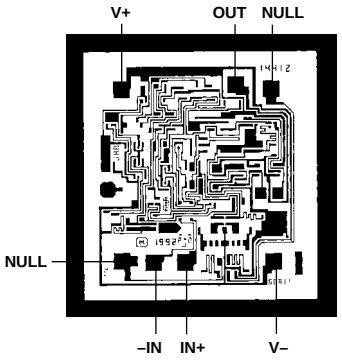
Package Type	θ_{JA}[3]	θ_{JC}	Units
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SOIC (S)	158	43	°C/W

NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]For supply voltages less than ±7 V, the absolute maximum input voltage is equal to the supply voltage. Maximum input current should not exceed 2 mA.
[3]θ_{JA} is specified for the worst case conditions, i.e., θ_{JA} is specified for device in socket for P-DIP packages; θ_{JA} is specified for device soldered in circuit board for SOIC packages.

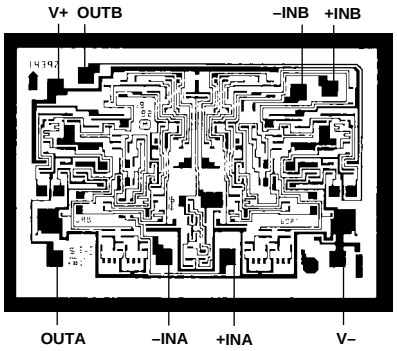
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
OP183GP	–40°C to +85°C	8-Pin Plastic DIP	N-8
OP183GS	–40°C to +85°C	8-Pin SOIC	SO-8
OP283GP	–40°C to +85°C	8-Pin Plastic DIP	N-8
OP283GS	–40°C to +85°C	8-Pin SOIC	SO-8

DICE CHARACTERISTICS



OP183 Die Size 0.058 X 0.063 Inch, 3,717 Sq. Mils Substrate (Die Backside) Is Connected to V–. Transistor Count, 30.



OP283 Die Size 0.063 X 0.092 Inch, 5,796 Sq. Mils Substrate (Die Backside) Is Connected to V–. Transistor Count, 55.

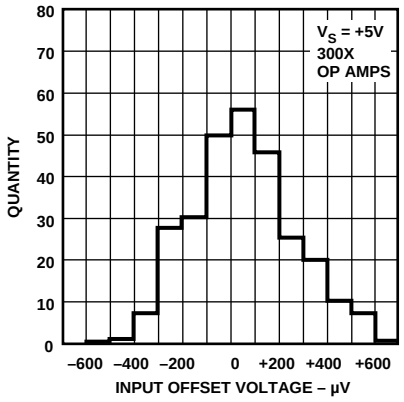


Figure 1. OP183 Input Offset Voltage Distribution @ +5 V

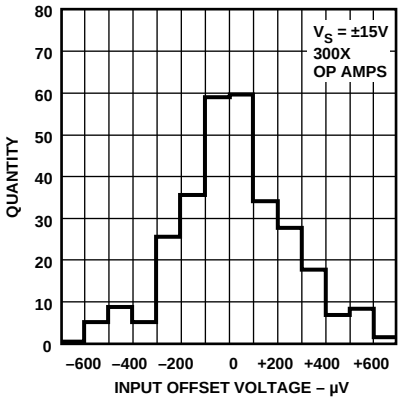


Figure 2. OP183 Input Offset Voltage Distribution @ ±15 V

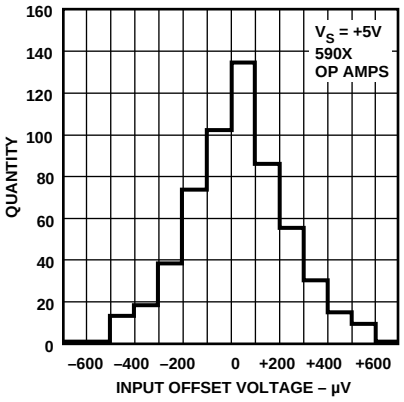


Figure 3. OP283 Input Offset Voltage Distribution @ +5 V

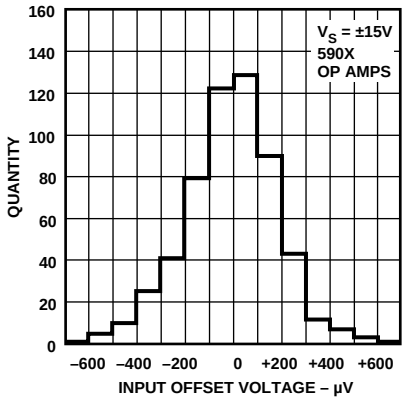


Figure 4. OP283 Input Offset Voltage Distribution @ ±15 V

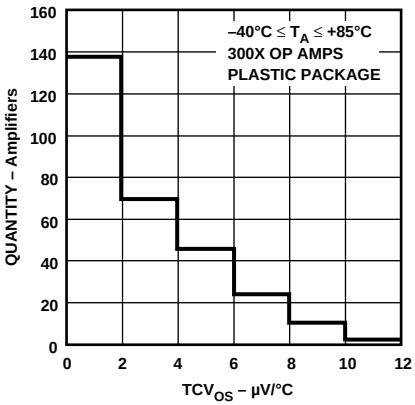


Figure 5. OP183 Input Offset Voltage Drift (TCV_{OS}) Distribution @ +5 V

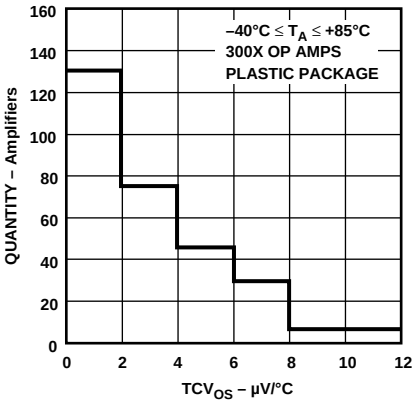


Figure 6. OP183 Input Offset Voltage Drift (TCV_{OS}) Distribution @ ±15 V

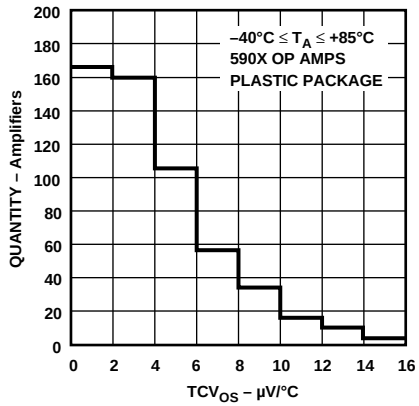


Figure 7. OP283 Input Offset Voltage Drift (TCV_{OS}) Distribution @ +5 V

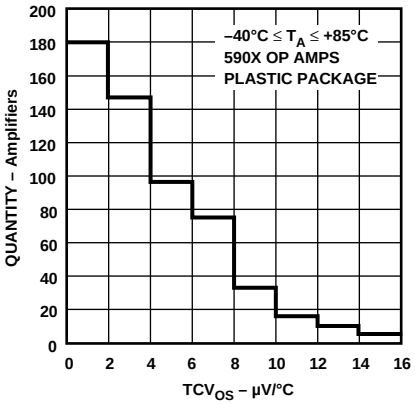


Figure 8. OP283 Input Offset Voltage Drift (TCV_{OS}) Distribution @ ±15 V

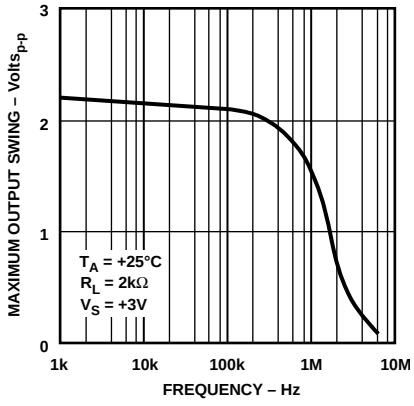


Figure 9. OP183/OP283 Maximum Output Swing vs. Frequency @ +3 V

OP183/OP283–Typical Characteristics

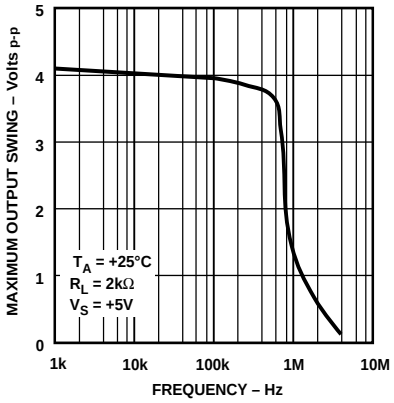


Figure 10. OP183/OP283 Maximum Output Swing vs. Frequency @ +5 V

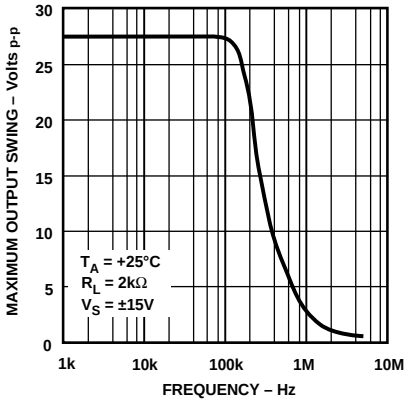


Figure 11. OP183/OP283 Maximum Output Swing vs. Frequency @ ±15 V

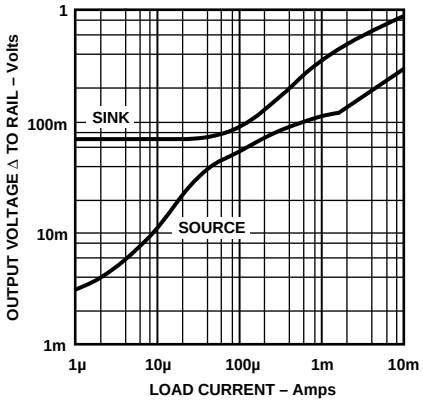


Figure 12. Output Voltage vs. Sink & Source Current

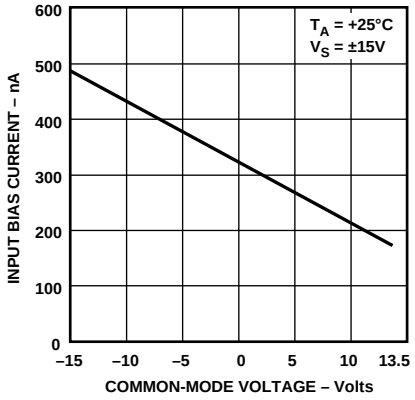


Figure 13. Input Bias Current vs. Common-Mode Voltage

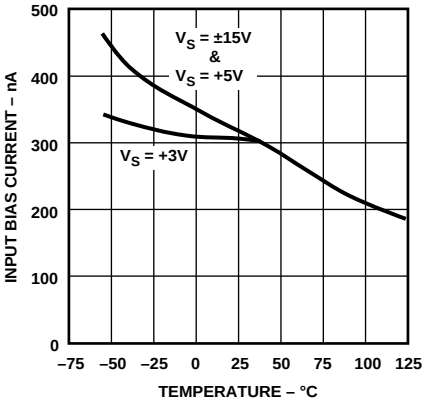


Figure 14. Input Bias Current vs. Temperature

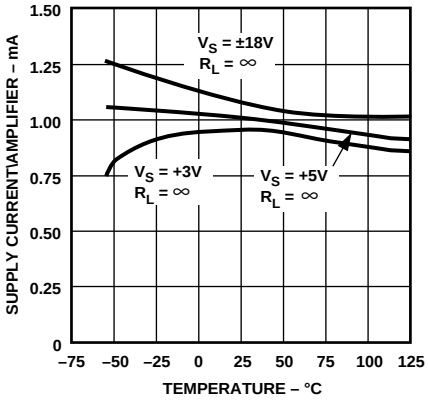


Figure 15. Supply Current per Amplifier vs. Temperature

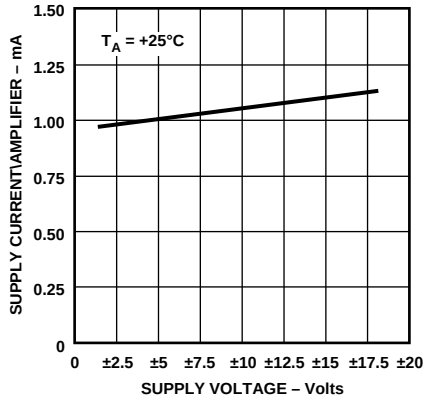


Figure 16. Supply Current per Amplifier vs. Supply Voltage

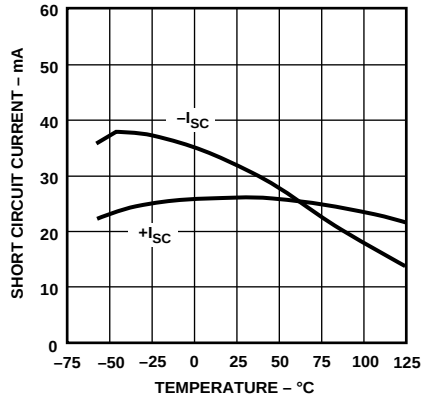


Figure 17. Short-Circuit Current vs. Temperature @ +5 V

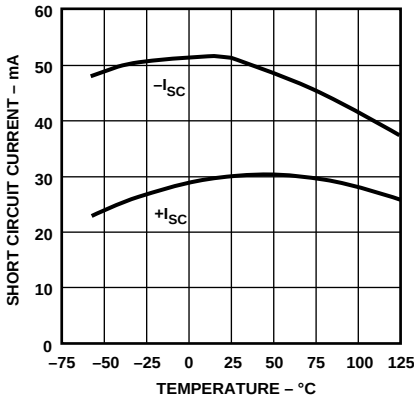


Figure 18. Short-Circuit Current vs. Temperature @ ±15 V

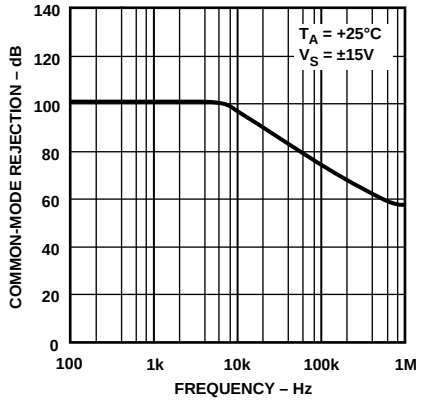


Figure 19. Common-Mode Rejection vs. Frequency

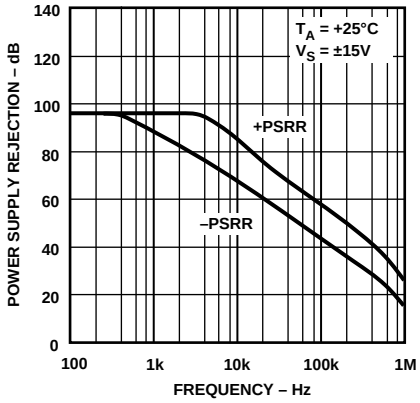


Figure 20. Power Supply Rejection vs. Frequency

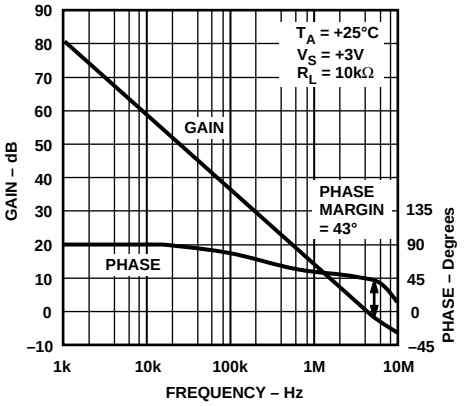


Figure 21. Open-Loop Gain and Phase vs. Frequency @ +3 V

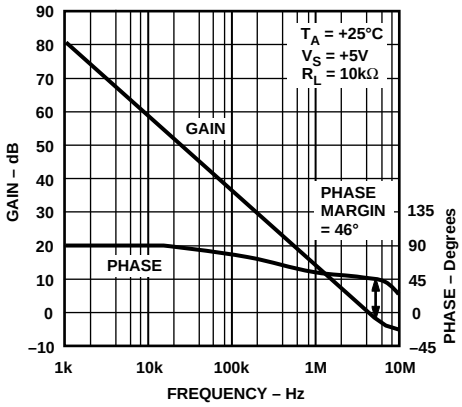


Figure 22. Open-Loop Gain and Phase vs. Frequency @ +5 V

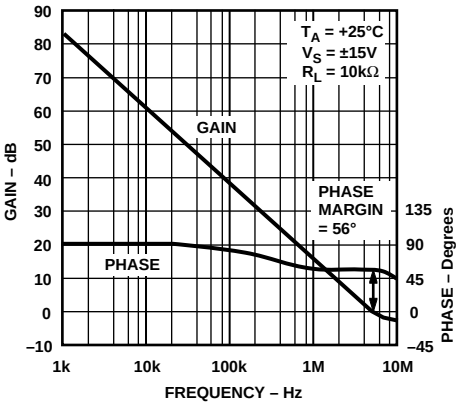


Figure 23. Open-Loop Gain and Phase vs. Frequency @ ±15 V

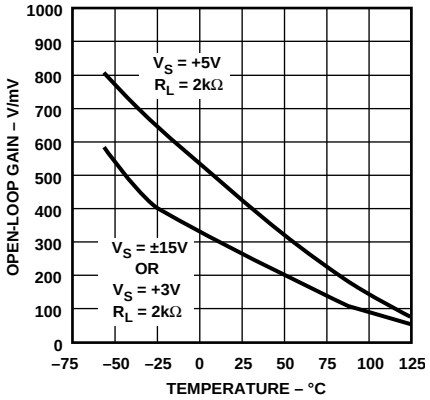


Figure 24. Open-Loop Gain vs. Temperature

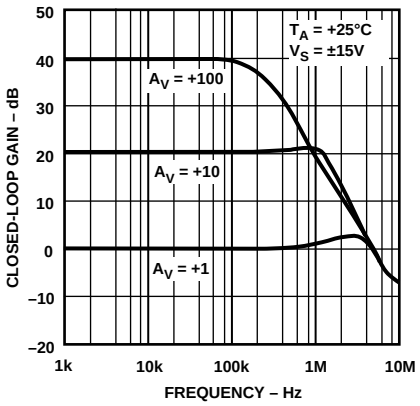


Figure 25. Closed-Loop Gain vs. Frequency

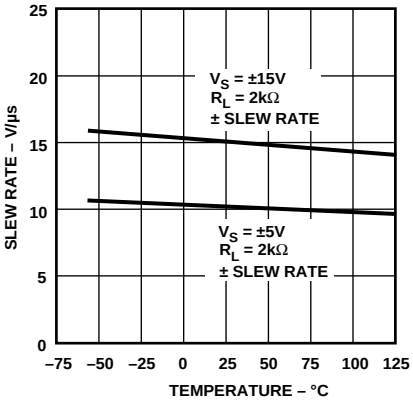


Figure 26. Slew Rate vs. Temperature

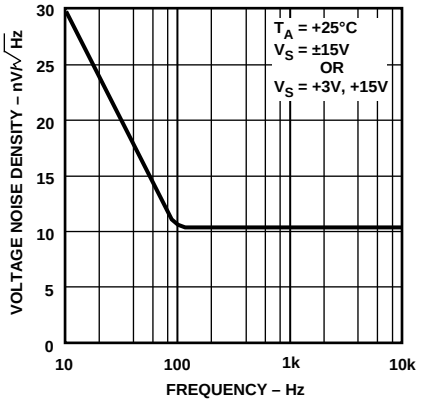


Figure 27. Voltage Noise Density vs. Frequency

OP183/OP283–Typical Characteristics

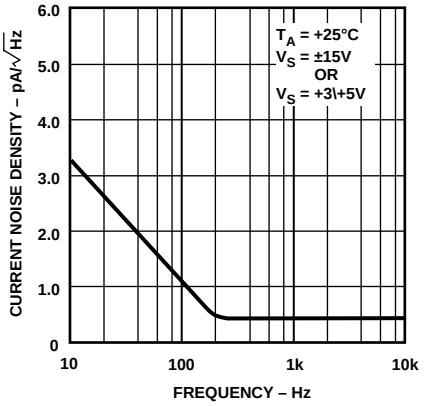


Figure 28. Current Noise Density vs. Frequency

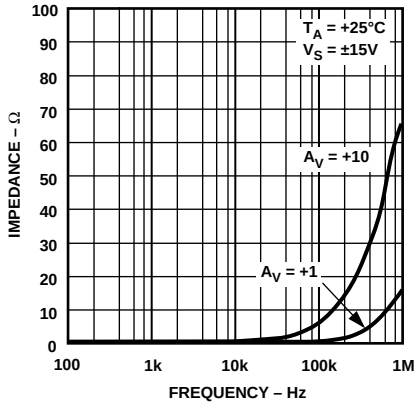


Figure 29. Closed-Loop Output Impedance vs. Frequency

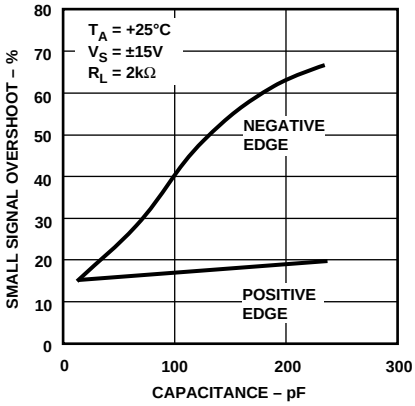


Figure 30. Small Signal Overshoot vs. Load Capacitance

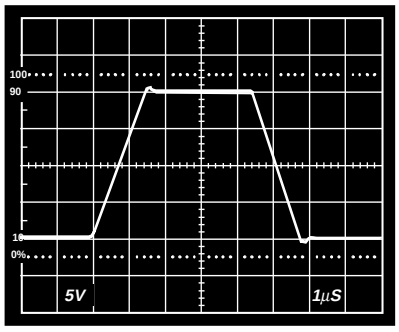


Figure 31. Large Signal Performance @ ±15 V

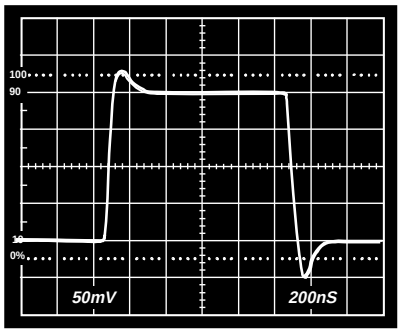


Figure 32. Small Signal Performance @ ±15 V

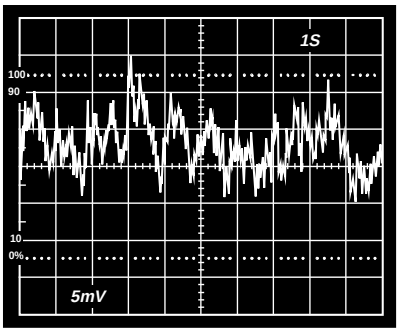


Figure 33. 0.1 Hz to 10 Hz Noise @ ± 2.5 V

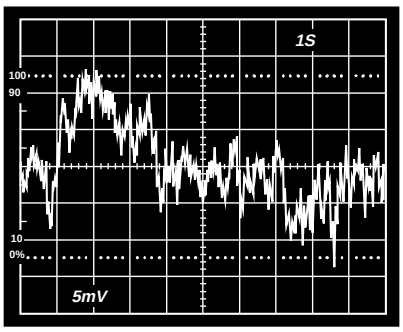


Figure 34. 0.1 Hz to 10 Hz Noise @ ±15 V

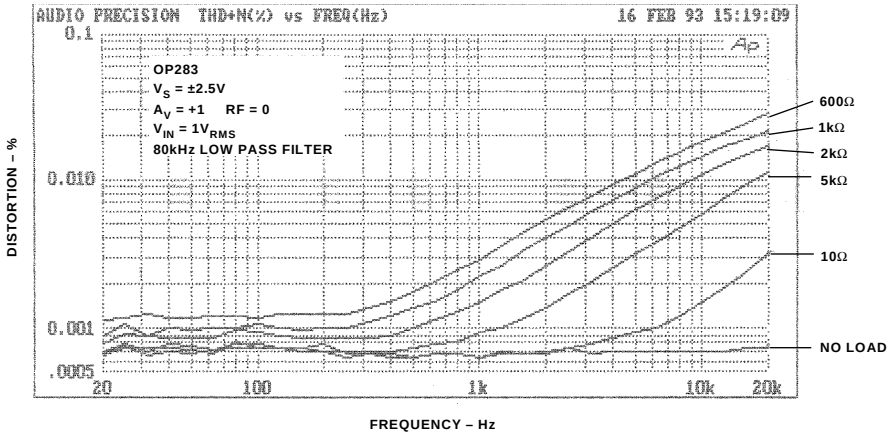


Figure 35. THD + Noise vs. Frequency for Various Loads

APPLICATIONS

OP183 Offset Adjust

Figure 36 shows how the OP183's offset voltage can be adjusted by connecting a potentiometer between Pins 1 and 5, and connecting the wiper to V_{EE}. The recommended value for the potentiometer is 10 kΩ. This will give an adjustment range of approximately ±1 mV. If larger adjustment span is desired, a 50 kΩ potentiometer will yield a range of ±2.5 mV.

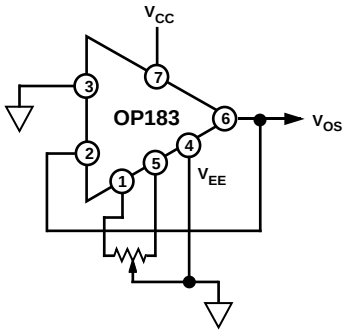


Figure 36. OP183 Offset Adjust

Phase Reversal

The OP183 family is protected against phase reversal as long as both of the inputs are within the range of the positive supply and the negative supply minus 0.6 volts. However if there is a possibility of either input going beyond these limits, then the inputs should be protected with a series resistor to limit input current to 2 mA.

Direct Access Arrangement

The OP183/OP283 can be used in a single supply Direct Access Arrangement (DAA) as is shown in Figure 37. This figure shows a portion of a typical DAA capable of operating from a single +5 volt supply and it should also work on +3 volt supplies with minor modifications. Amplifiers A2 and A3 are configured so that the transmit signal TXA is inverted by A2 and is not inverted by A3. This arrangement drives the transformer differentially so that the drive to the transformer is effectively doubled over a single amplifier arrangement. This application takes advantage of the OP183/283's ability to drive capacitive loads, and to save power in single supply applications.

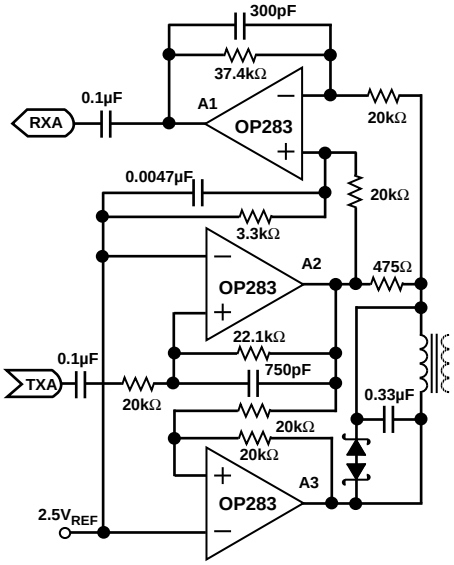


Figure 37. Direct Access Arrangement

+5 Volt Only Stereo DAC for Multimedia

The OP283's low noise and single supply capability are ideally suited for stereo DAC audio reproduction or sound synthesis applications such as multimedia systems. Figure 38 shows an 18-bit stereo DAC output setup that is powered from a single +5 volt supply. The low noise preserves the 18-bit dynamic range of the AD1868. For DACs that operate on dual supplies, the OP283 can also be powered from the same supplies.

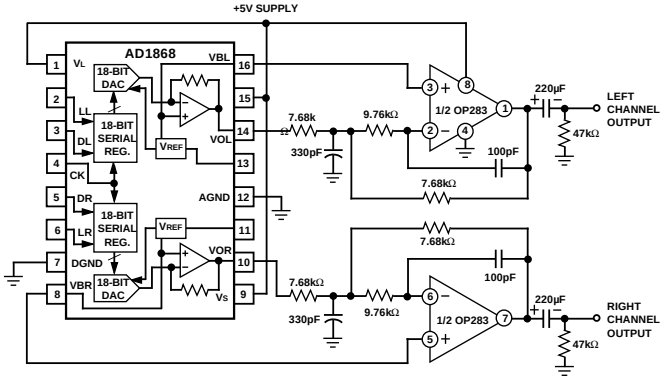


Figure 38. +5 Volt Only 18-Bit Stereo DAC

Low Voltage Headphone Amplifiers

Figure 39 shows a stereo headphone output amplifier for the AD1849 16-bit SoundPort® Stereo Codec device. The pseudo-reference voltage is derived from the common-mode voltage generated internally by the AD1849, thus providing a convenient bias for the headphone output amplifiers.

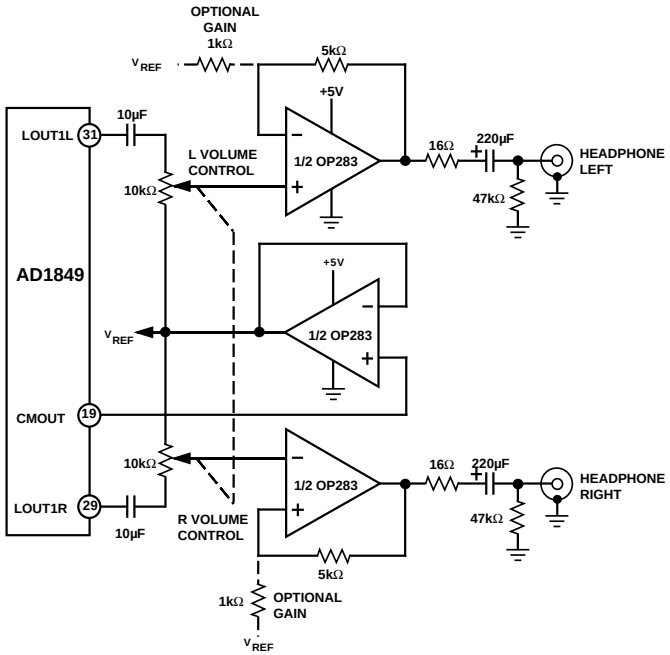


Figure 39. Headphone Output Amplifier for Multimedia Sound Codec

SoundPort is a registered trademark of Analog Devices Inc.

Low Noise Microphone Amplifier for Multimedia

The OP183 family is ideally suited as a low noise microphone preamp for low voltage audio applications. Figure 40 shows a gain of 100 stereo preamp for the AD1849 16-bit SoundPort Stereo Codec chip. The common-mode output buffer serves as a "phantom power" driver for the microphones.

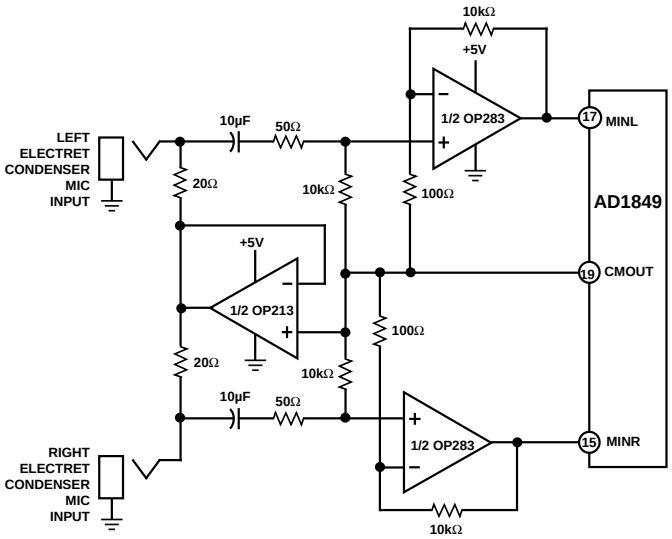


Figure 40. Low Noise Stereo Microphone Amplifier for Multimedia Sound CODEC

A +3 Volt 50 Hz/60 Hz Active Notch Filter with False Ground

To process ac signals, it may be easier to use a false-ground bias rather than the negative supply as a reference ground. This would reject the power-line frequency interference which oftentimes can obscure low frequency physiological signals, such as heart rates, blood pressures, EEGs, ECGs, et cetera.

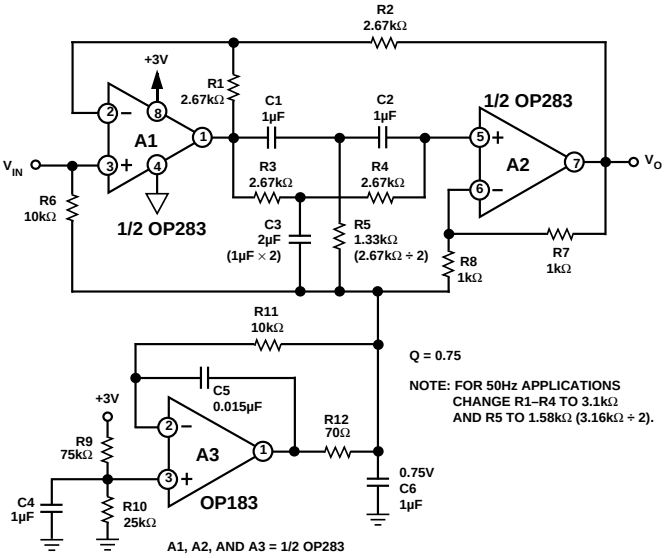


Figure 41. +3 Volt Supply 50 Hz/60 Hz Notch Filter with Pseudo Ground

Figure 41 shows a 50 Hz/60 Hz active notch filter for eliminating line noise in patient monitoring equipment. It has several kilohertz bandwidth and is not sensitive to false-ground perturbations. The simple false-ground circuit shown achieves good rejection of low frequency interference using standard off-the-shelf components.

Amplifier A3 biases A1 and A2 to the middle of their input common-mode range. When operating on a +3 V supply, the center of the OP283's common-mode range is 0.75 V. This notch filter effectively squelches 60 Hz pickup at a filter Q of 0.75. To reject 50 Hz interference, simply change the resistors in the twin-T section (R1 through R5) from 2.67 kΩ to 3.16 kΩ.

The filter section uses an OP283 dual op amp in a twin-T configuration whose frequency selectivity is very sensitive to the relative matching of the capacitors and resistors in the twin-T section. Mylar is the material of choice for the capacitors, and the relative matching of the capacitors and resistors determines the filter's pass band symmetry. Using 1% resistors and 5% capacitors produces satisfactory results.

A Low Voltage Frequency Synthesizer for Wireless Transceiver

The OP183's low noise and the low voltage operation capability serves well for the loop filter of a frequency synthesizer. Figure 42 shows a typical application in a radio transceiver. The phase noise performance of the synthesizer depends on low noise contribution from each component in the loop as the noise is amplified by the frequency division factor of the prescaler.

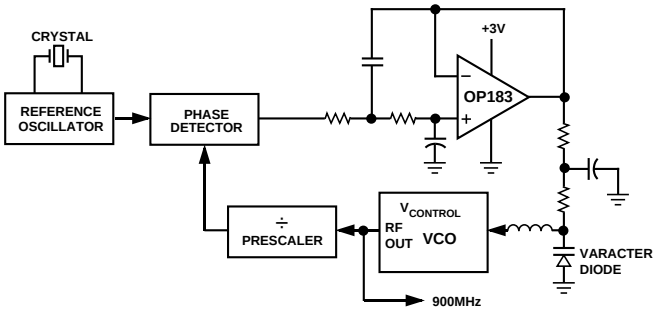


Figure 42. A Low Voltage Frequency Synthesizer for a Wireless Transceiver

The resistors used in the low-pass filter should be of low to moderate values to reduce noise contribution due to the input bias current as well as the resistors themselves. The filter cutoff frequency should be chosen to optimize the loop constant.

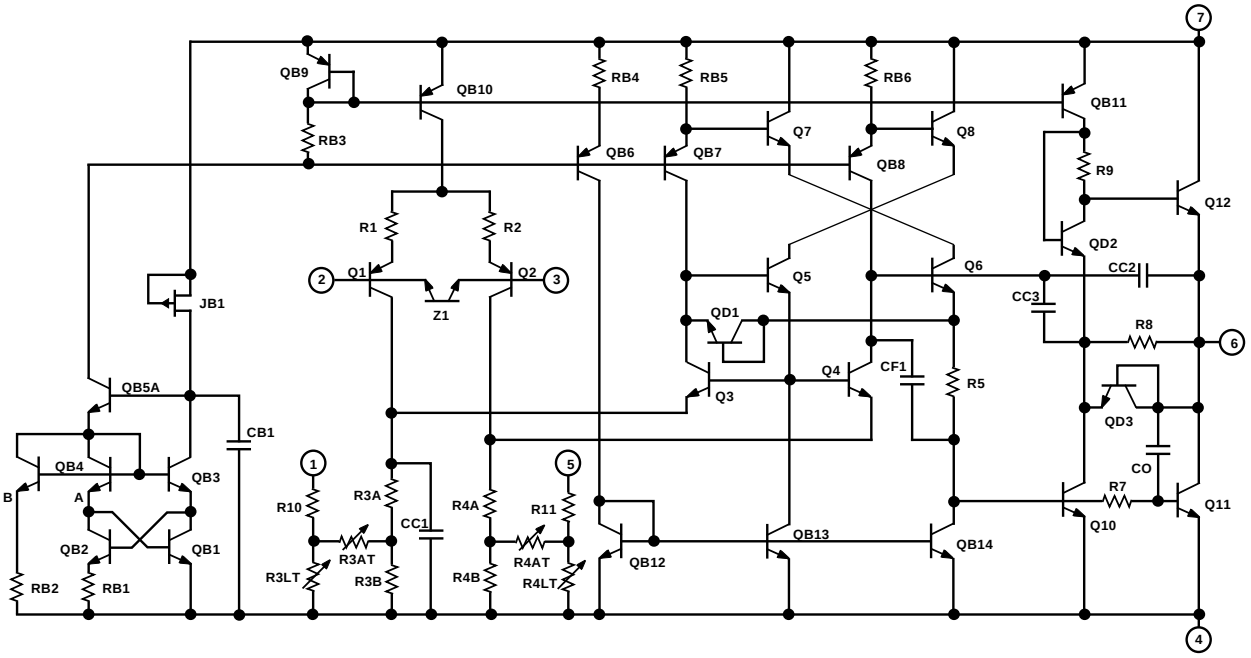


Figure 43. OP183 Simplified Schematic

```
* OP283 SPICE Macro-model                    Rev. A, 9/93
*                                            JCB/ADI
*
* Copyright 1993 by Analog Devices
*
* Refer to "README.DOC" file for License Statement.
* Use of  this model indicates your acceptance of the terms and
* provisions in the License Statement.
*
* Node assignments
*                  noninverting input
*                  |  inverting input
*                  |  |  positive supply
*                  |  |  |  negative supply
*                  |  |  |  |  output
*                  |  |  |  |  |
.SUBCKT OP283 2  1  99  50  45
*
* INPUT STAGE AND POLE AT 600 kHz
*
I1        99      8       1E-4
Q1        4       1       6       QP
Q2        5       3       7       QP
CIN       1       2       1.5PF
R1        50      4       1591
R2        50      5       1591
C1        4       5       83.4E-12
R3        6       8       1075
R4        7       8       1075
IOS       1       2       12.5E-9
EOS       3       2       POLY(1) (15,98) 25E-6 1
DC1       2       36      DZ
DC2       1       36      DZ
*
* GAIN STAGE AND DOMINANT POLE AT 10 Hz
*
EREF      98      0       POLY(2) (99,0) (50,0) 0 0.5 0.5
G1        98      9       (4,5) 6.28E-4
R5        9       98      1.59E9
C2        9       98      10E-12
D1        9       10      DX
D2        11      9       DX
E1        10      98      POLY(1)  99  98  -1.35  1.03
V2        50      11      –0.63
*
* COMMON MODE STAGE WITH ZERO AT 353 Hz
*
ECM       14      98      POLY(2) (1,98) (2,98) 0 3.5 3.5
R7        14      15      1E6
C4        14      15      3.75E-11
R8        15      98      1
*
*POLE AT 20 MHz
*
GP2       98      31      (9,98) 1E-6
RP2       31      98      1E6
CP2       31      98      7.96E-15
*
*ZERO AT  1.5 MHz
*
EZ1       32      98      (31,98) 1E6
RZ1       32      33      1E6
RZ2       33      98      1
CZ1       32      33      106E-15
*
*POLE AT 10 MHz
*
GP10      98      40      (33,98) 1E-6
RP10      40      98      1E6
CP10      40      98      15.9E-15
*
* OUTPUT STAGE
*
RO1       99      45      140
```

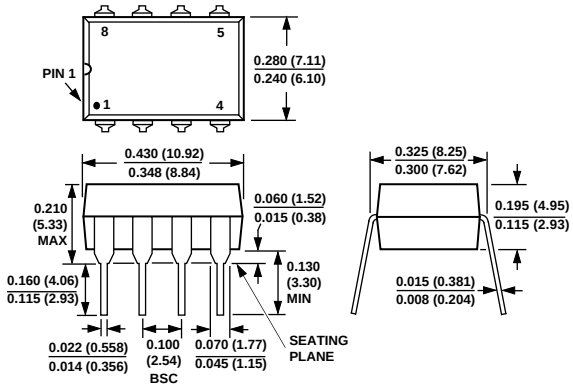
```
RO2   45   50   140                          D10   42   40   DX
G7    45   99   (99,40)      7.14E-3         V5    41   45   1.2
G8    50   45   (40,50)      7.14E-3         V6    45   42   1.5
G9    98   60   (45,40)      7.14E-3         *
D7    60   61   DX                           * MODELS USED
D8    62   60   DX                           *
V7    61   98   DC 0                         .MODEL DX D
V8    98   62   DC 0                         .MODEL DZ D(IS=1E-15 BV=7.0)
GSY   99   50   (99,50)5E-6                  .MODEL QP PNP(BF=143)
FSY   99   50   POLY(2) V7 V8 1.075E-3  1  1 .ENDS
D9    40   41   DX
```

C1858a–3–2/96

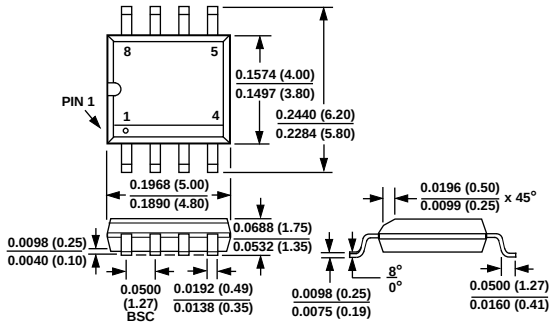
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead Plastic DIP (N-8)



8-Lead Narrow-Body SO (SO-8)



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