

NXP ACTT8B-800C0 Thyristor datasheet

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AC Thyristor Triac power switch in a SOT404 (D2PAK) surface mountable plastic package with self-protective clamping capabilities against low and high energy transients.

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ACTT8B-800C0

AC Thyristor Triac power switch

12 March 2014

Product data sheet

1. General description

AC Thyristor Triac power switch in a SOT404 (D2PAK) surface mountable plastic package with self-protective clamping capabilities against low and high energy transients.

2. Features and benefits

- Clamping structure ensuring safe high over-voltage withstand capability
- High minimum I_{GT} for guaranteed immunity to gate noise
- Full cycle AC conduction
- Over-voltage withstand capability to IEC 61000-4-5
- Pin compatible with standard triacs
- Planar passivated for voltage ruggedness and reliability
- Protective self turn-on capability for high energy transients
- Safe clamping capability for low energy over-voltage transients
- Less sensitive gate for high noise immunity
- Surface mountable package
- Triggering in three quadrants only
- Very high immunity to false turn-on by dV/dt

3. Applications

- AC fan, pump and compressor controls
- Highly inductive, resistive and safety loads
- Large and small appliances (White Goods)
- Reversing induction motor controls

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	-	800	V
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5	-	-	80	A
T_j	junction temperature		-	-	125	$^{\circ}\text{C}$
$I_{T(\text{RMS})}$	RMS on-state current	full sine wave; $T_{mb} \leq 105\text{ }^{\circ}\text{C}$; Fig. 1 ; Fig. 2 ; Fig. 3	-	-	8	A



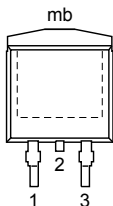
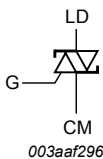
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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{PP}	peak pulse voltage	T _J = 25 °C; non-repetitive, off-state; Fig. 6	-	-	2	kV
Static characteristics						
I _{GT}	gate trigger current	V _D = 12 V; I _T = 100 mA; LD+ G+; T _J = 25 °C; Fig. 8	5	-	30	mA
		V _D = 12 V; I _T = 100 mA; LD+ G-; T _J = 25 °C; Fig. 8	5	-	30	mA
		V _D = 12 V; I _T = 100 mA; LD- G-; T _J = 25 °C; Fig. 8	5	-	30	mA
V _{CL}	clamping voltage	I _{CL} = 0.1 mA; t _p = 1 ms; T _J = 25 °C	850	-	-	V
Dynamic characteristics						
dV _D /dt	rate of rise of off-state voltage	V _{DM} = 536 V; T _J = 125 °C; (V _{DM} = 67% of V _{DRM}); exponential waveform; gate open circuit	2000	-	-	V/μs
dI _{com} /dt	rate of change of commutating current	V _D = 400 V; T _J = 125 °C; I _{T(RMS)} = 8 A; dV _{com} /dt = 20 V/μs; (snubberless condition); gate open circuit	8	-	-	A/ms

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	CM	common	 <p>D2PAK (SOT404)</p>	
2	LD	load		
3	G	gate		
mb	LD	mounting base; load		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
ACTT8B-800C0	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

7. Marking

Table 4. Marking codes

Type number	Marking code
ACTT8B-800C0	ACTT8B-800C0

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 105\text{ °C}$; Fig. 1 ; Fig. 2 ; Fig. 3	-	8	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(\text{init})} = 25\text{ °C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5	-	80	A
		full sine wave; $T_{j(\text{init})} = 25\text{ °C}$; $t_p = 16.7\text{ ms}$	-	88	A
I^2t	I^2t for fusing	$t_p = 10\text{ ms}$; sine-wave pulse	-	32	A^2s
dI_T/dt	rate of rise of on-state current	$I_T = 12\text{ A}$; $I_G = 0.2\text{ A}$; $dI_G/dt = 0.2\text{ A}/\mu s$	-	100	$A/\mu s$
I_{GM}	peak gate current	$t = 20\text{ }\mu s$	-	2	A
P_{GM}	peak gate power		-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.5	W
T_{stg}	storage temperature		-40	150	$^{\circ}C$
T_j	junction temperature		-	125	$^{\circ}C$
V_{PP}	peak pulse voltage	$T_j = 25\text{ °C}$; non-repetitive, off-state; Fig. 6	-	2	kV

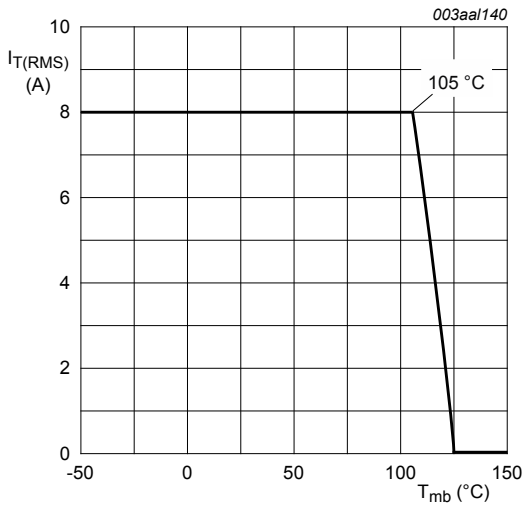


Fig. 1. RMS on-state current as a function of mounting base temperature; maximum values

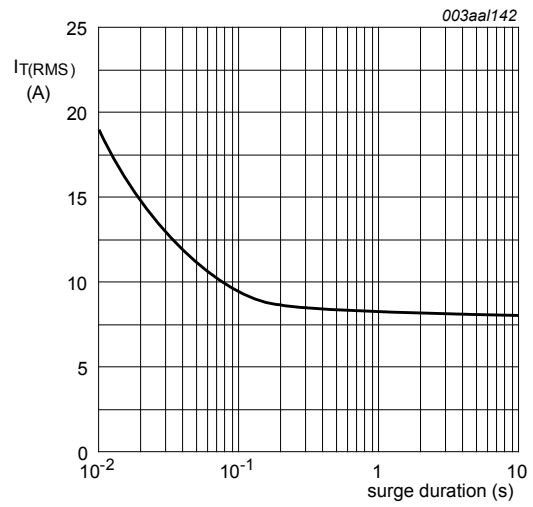


Fig. 2. RMS on-state current as a function of surge duration; maximum values
 f = 50 Hz; T_{mb} = 105 °C

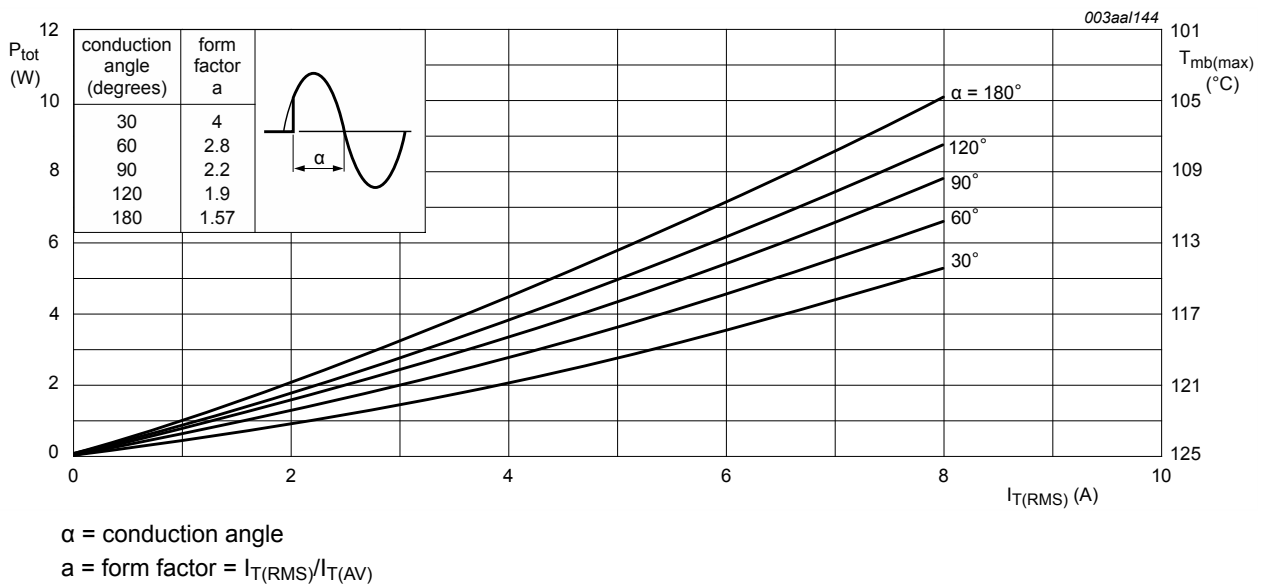


Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

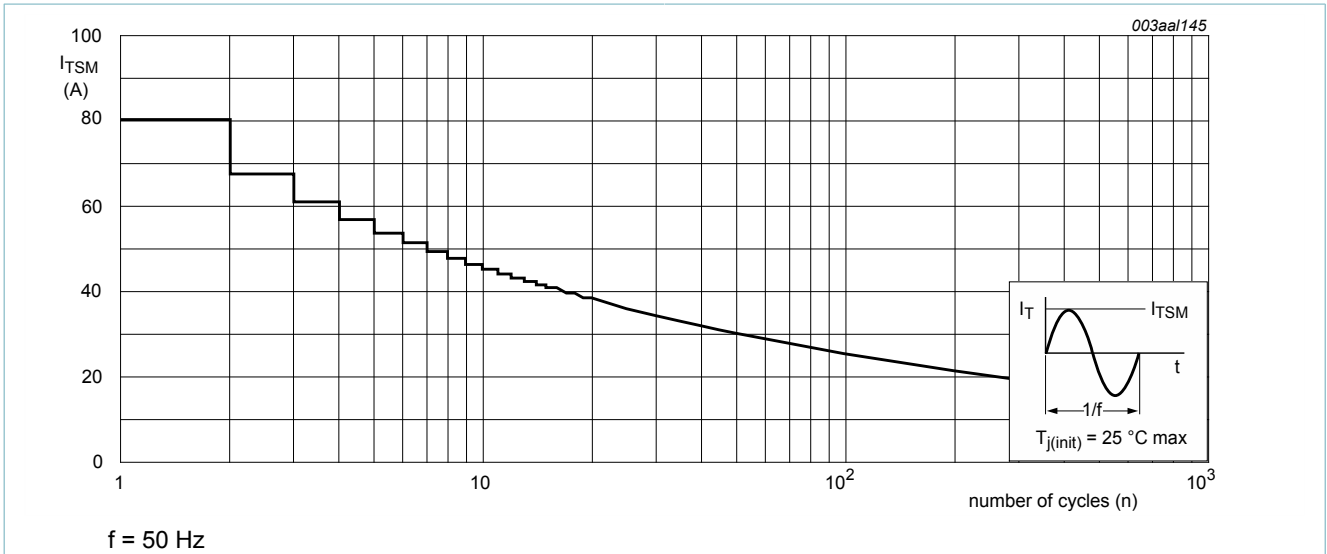


Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

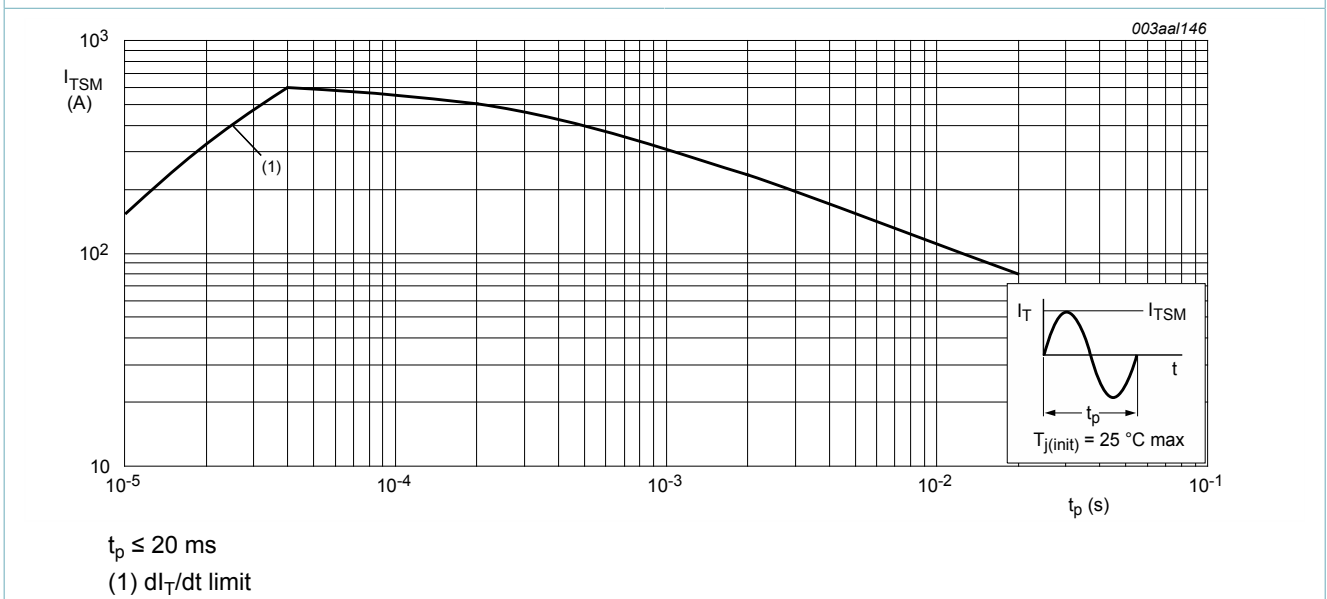


Fig. 5. Non-repetitive peak on-state current as a function of pulse width; maximum values

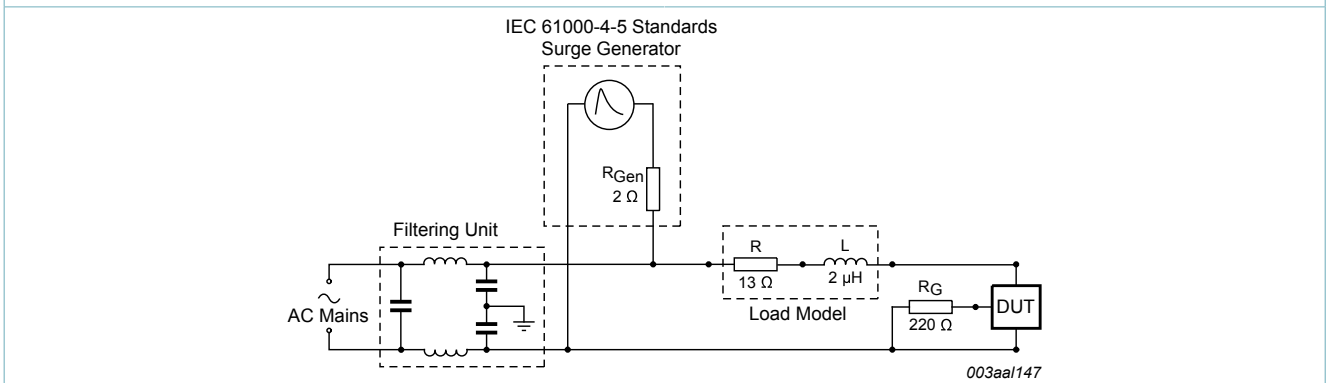
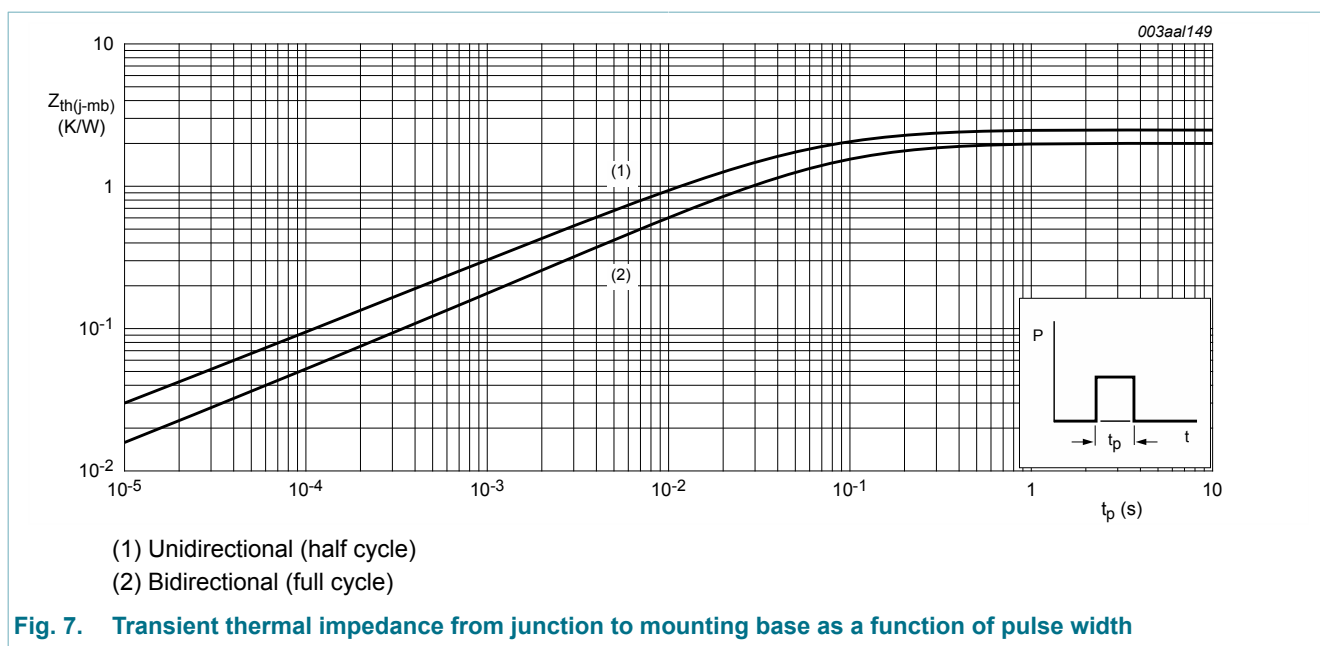


Fig. 6. Test circuit for inductive and resistive loads with conditions equivalent to IEC 61000-4-5

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R _{th(j-mb)}	thermal resistance from junction to mounting base	full cycle; Fig. 7	-	-	2	K/W
		half cycle; Fig. 7	-	-	2.4	K/W
R _{th(j-a)}	thermal resistance from junction to ambient	in free air; printed circuit board (FR4) mounted	-	55	-	K/W

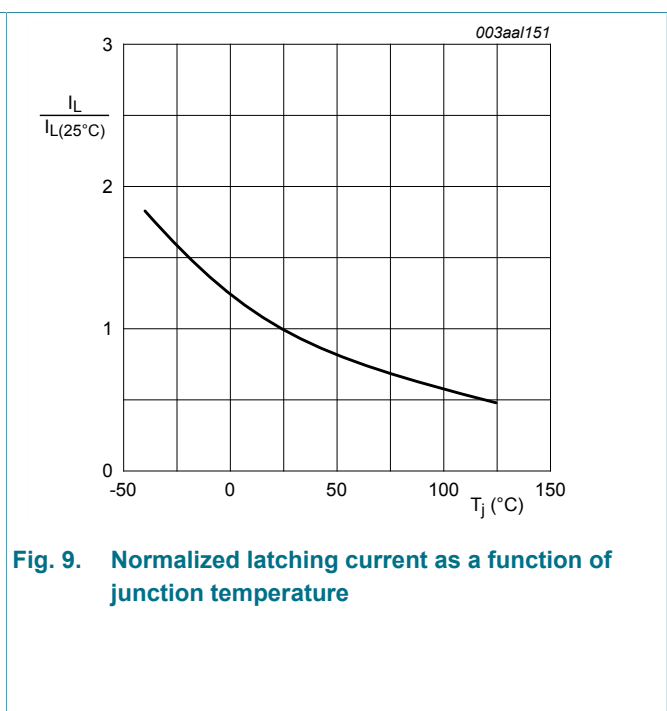
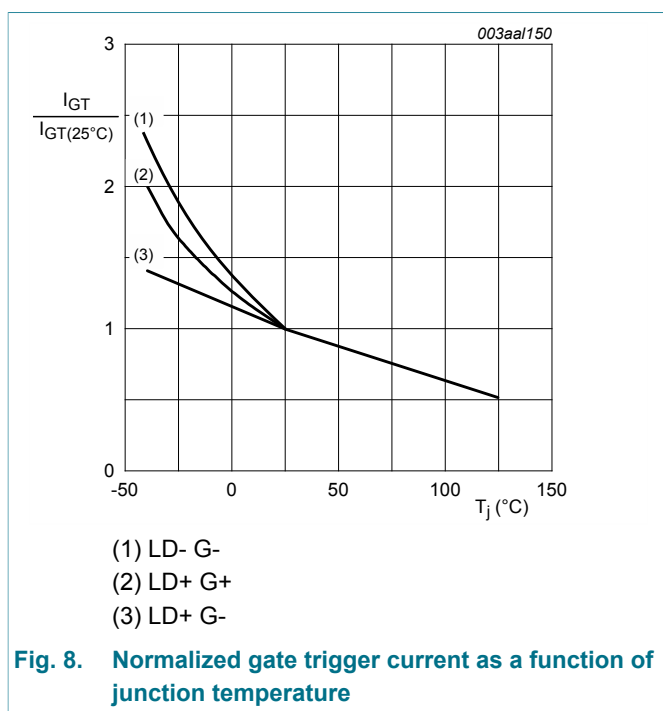


10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I _{GT}	gate trigger current	V _D = 12 V; I _T = 100 mA; LD+ G+; T _j = 25 °C; Fig. 8	5	-	30	mA
		V _D = 12 V; I _T = 100 mA; LD+ G-; T _j = 25 °C; Fig. 8	5	-	30	mA
		V _D = 12 V; I _T = 100 mA; LD- G-; T _j = 25 °C; Fig. 8	5	-	30	mA
I _L	latching current	V _D = 12 V; I _G = 100 mA; LD+ G+; T _j = 25 °C; Fig. 9	-	-	50	mA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		$V_D = 12\text{ V}; I_G = 100\text{ mA}; \text{LD+ G-}; T_j = 25\text{ }^\circ\text{C}; \text{Fig. 9}$	-	-	70	mA
		$V_D = 12\text{ V}; I_G = 100\text{ mA}; \text{LD- G-}; T_j = 25\text{ }^\circ\text{C}; \text{Fig. 9}$	-	-	50	mA
I_H	holding current	$V_D = 12\text{ V}; T_j = 25\text{ }^\circ\text{C}; \text{Fig. 10}$	-	-	35	mA
V_T	on-state voltage	$I_T = 10\text{ A}; T_j = 25\text{ }^\circ\text{C}; \text{Fig. 11}$	-	1.3	1.5	V
V_{GT}	gate trigger voltage	$V_D = 12\text{ V}; I_T = 100\text{ mA}; T_j = 25\text{ }^\circ\text{C}; \text{Fig. 12}$	-	0.8	1	V
		$V_D = 400\text{ V}; I_T = 100\text{ mA}; T_j = 125\text{ }^\circ\text{C}; \text{Fig. 12}$	0.2	0.45	-	V
I_D	off-state current	$V_D = 800\text{ V}; T_j = 25\text{ }^\circ\text{C}$	-	-	10	μA
		$V_D = 800\text{ V}; T_j = 125\text{ }^\circ\text{C}$	-	-	0.5	mA
V_{CL}	clamping voltage	$I_{CL} = 0.1\text{ mA}; t_p = 1\text{ ms}; T_j = 25\text{ }^\circ\text{C}$	850	-	-	V
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 536\text{ V}; T_j = 125\text{ }^\circ\text{C}; (V_{DM} = 67\% \text{ of } V_{DRM}); \text{exponential waveform; gate open circuit}$	2000	-	-	$\text{V}/\mu\text{s}$
di_{com}/dt	rate of change of commutating current	$V_D = 400\text{ V}; T_j = 125\text{ }^\circ\text{C}; I_{T(RMS)} = 8\text{ A}; dV_{com}/dt = 20\text{ V}/\mu\text{s}; (\text{snubberless condition}); \text{gate open circuit}$	8	-	-	A/ms



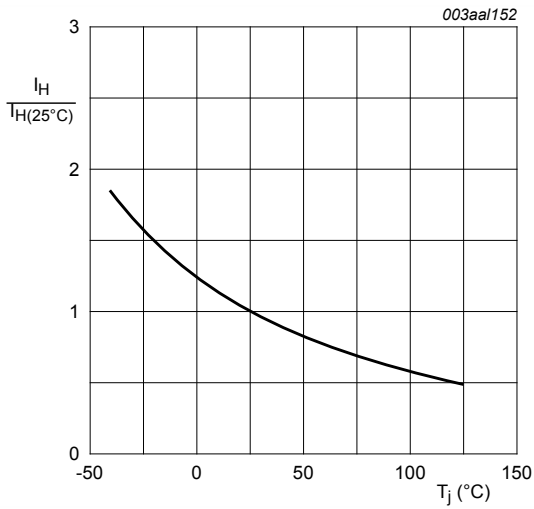
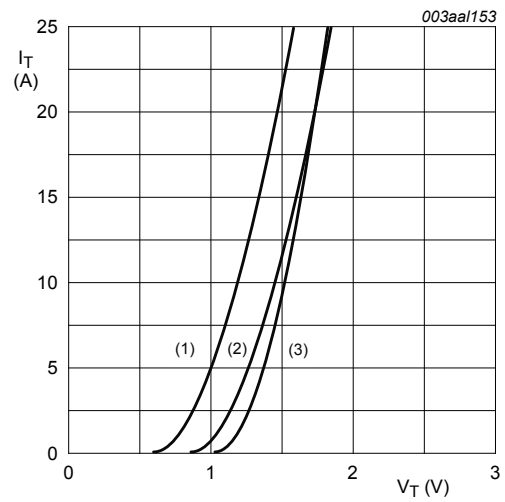


Fig. 10. Normalized holding current as a function of junction temperature



$V_o = 1.103 \text{ V}; R_s = 0.034 \Omega$
 (1) $T_j = 125^\circ\text{C}$; typical values
 (2) $T_j = 125^\circ\text{C}$; maximum values
 (3) $T_j = 25^\circ\text{C}$; maximum values

Fig. 11. On-state current as a function of on-state voltage

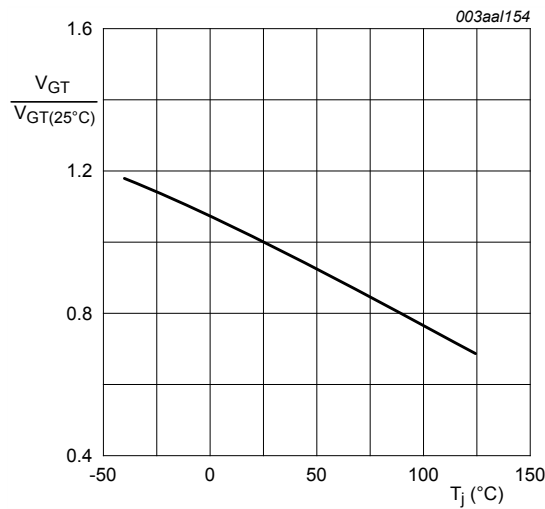


Fig. 12. Normalized gate trigger voltage as a function of junction temperature

11. Package outline

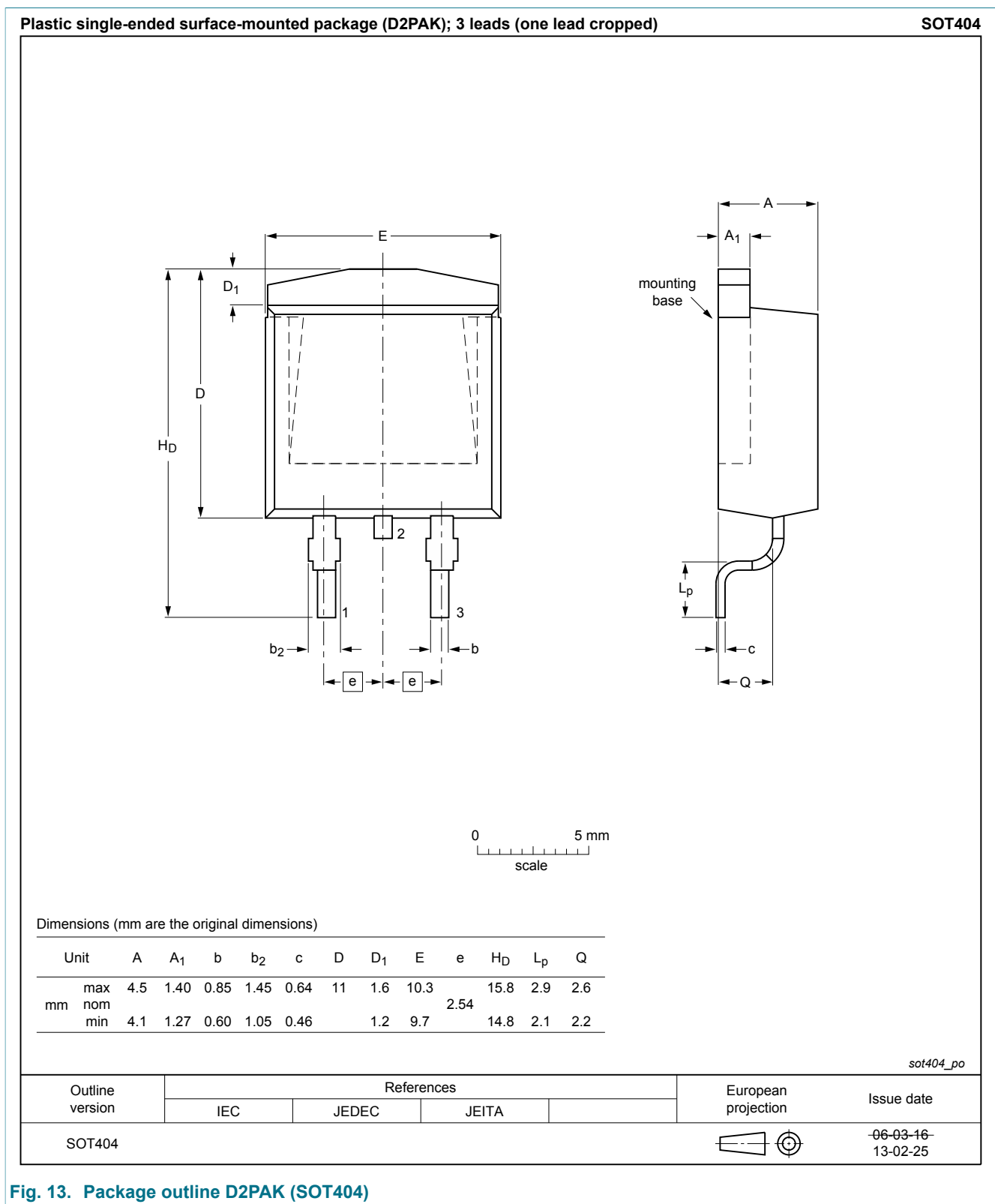


Fig. 13. Package outline D2PAK (SOT404)

12. Soldering

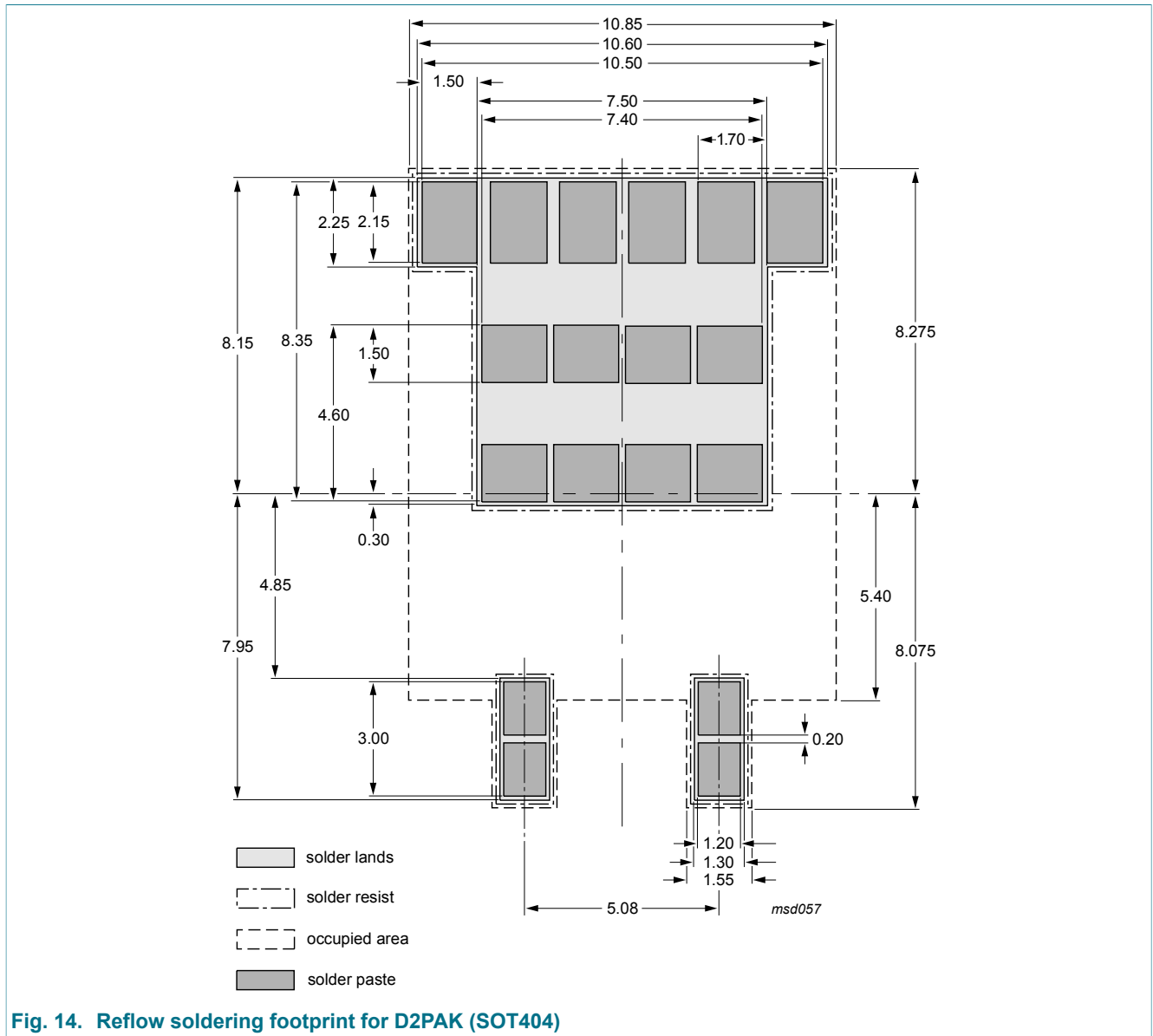


Fig. 14. Reflow soldering footprint for D2PAK (SOT404)

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Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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14. Contents

1	General description	1
2	Features and benefits	1
3	Applications	1
4	Quick reference data	1
5	Pinning information	2
6	Ordering information	2
7	Marking	3
8	Limiting values	3
9	Thermal characteristics	6
10	Characteristics	6
11	Package outline	9
12	Soldering	10
13	Legal information	11
13.1	Data sheet status	11
13.2	Definitions	11
13.3	Disclaimers	11
13.4	Trademarks	12

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Date of release: 12 March 2014