

SN54ABT16646, SN74ABT16646 16-BIT BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCBS212D – JUNE 1992 – REVISED JULY 1999

- Members of the Texas Instruments **Widebus™** Family
- State-of-the-Art **EPIC-II B™** BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs (–32-mA I_{OH} , 64-mA I_{OL})
- Package Options Include Plastic Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

description

The 'ABT16646 devices consist of bus-transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers.

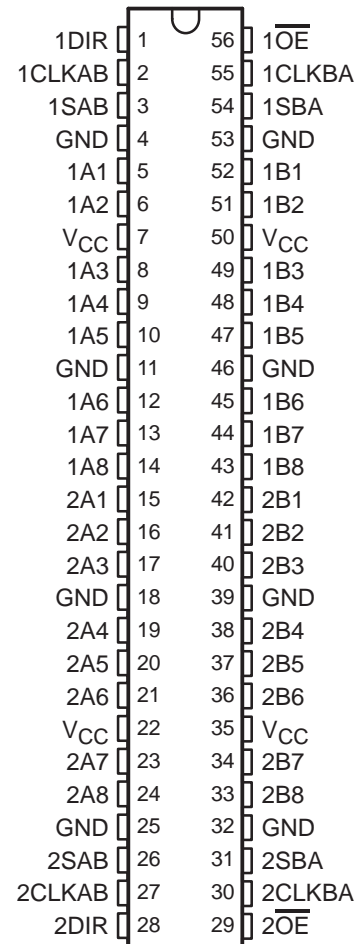
These devices can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'ABT16646 devices.

Output-enable (\overline{OE}) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. The direction control (DIR) determines which bus receives data when \overline{OE} is low. In the isolation mode (\overline{OE} high), A data can be stored in one register and/or B data can be stored in the other register.

When an output function is disabled, the input function is still enabled and can be used to store and transmit data. Only one of the two buses, A or B, can be driven at a time.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

SN54ABT16646 . . . WD PACKAGE SN74ABT16646 . . . DGG OR DL PACKAGE (TOP VIEW)



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SN54ABT16646, SN74ABT16646

16-BIT BUS TRANSCEIVERS AND REGISTERS

WITH 3-STATE OUTPUTS

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description (continued)

The SN54ABT16646 is characterized for operation over the full military temperature range of -55°C to 125°C .
The SN74ABT16646 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION
$\overline{\text{OE}}$	DIR	CLKAB	CLKBA	SAB	SBA	A1–A8	B1–B8	
X	X	↑	X	X	X	Input	Unspecified	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	H or L	H or L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B Bus
L	H	H or L	X	H	X	Input	Output	Stored A data to bus

† The data-output functions can be enabled or disabled by various signals at $\overline{\text{OE}}$ or DIR. Data-input functions always are enabled, i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

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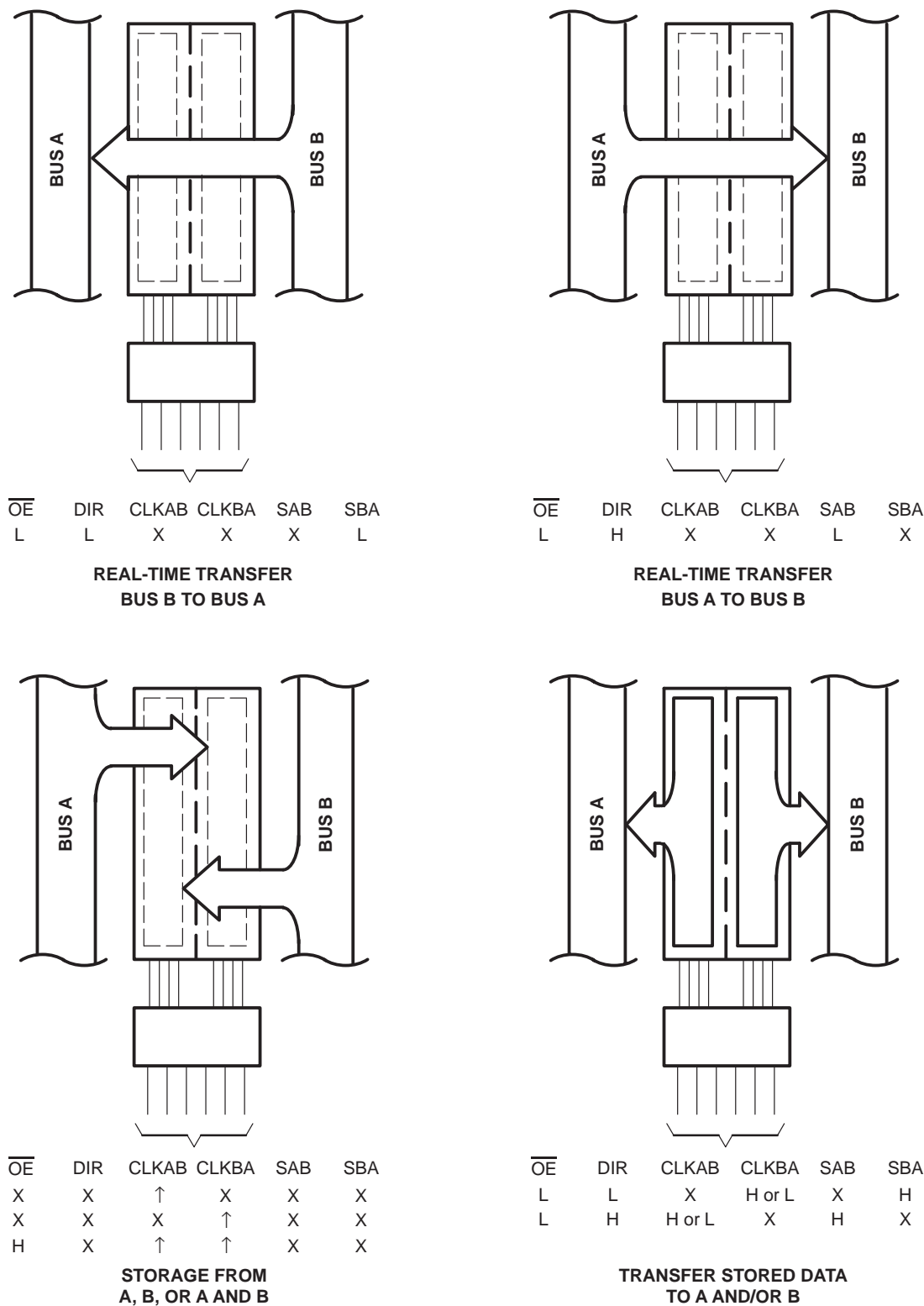


Figure 1. Bus-Management Functions

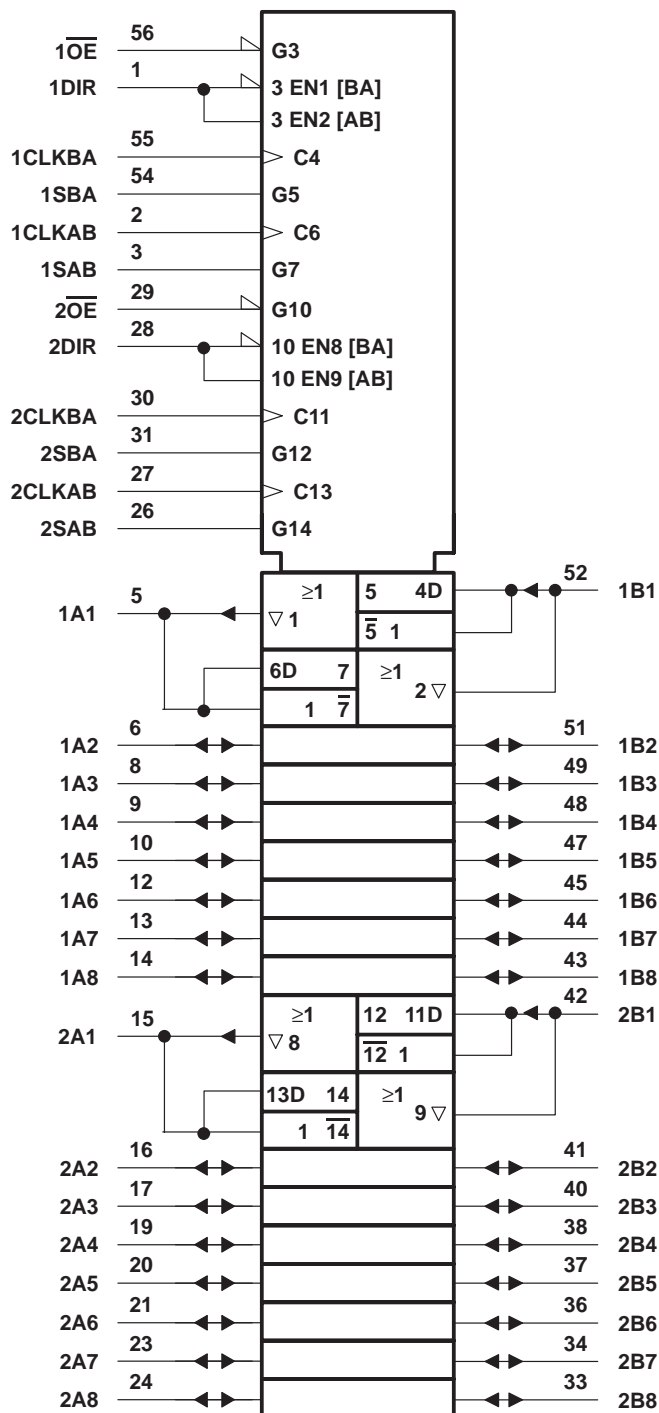
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



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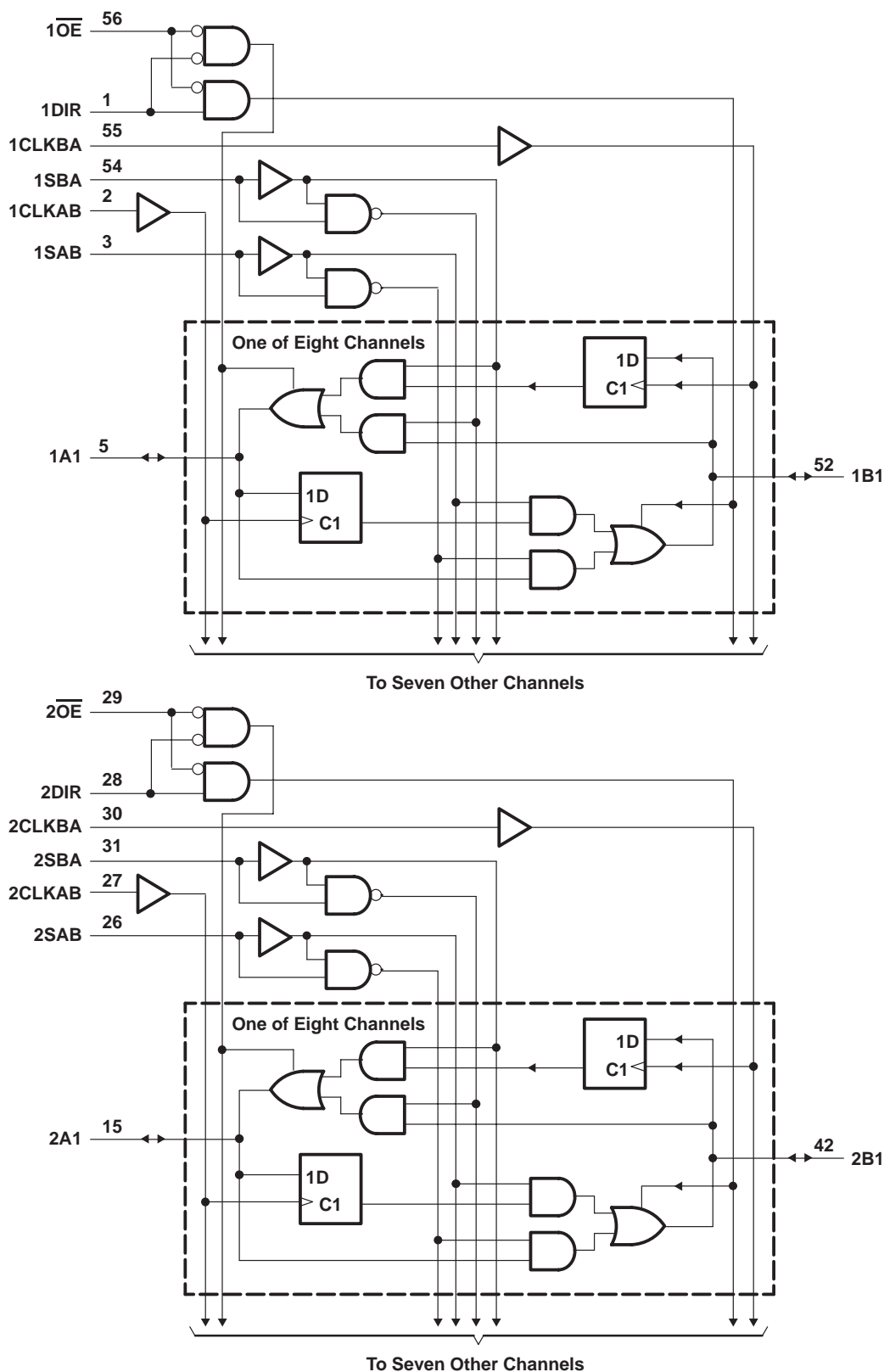
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logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O	–0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABT16646	96 mA
SN74ABT16646	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package	81°C/W
DL package	74°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		SN54ABT16646		SN74ABT16646		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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16-BIT BUS TRANSCEIVERS AND REGISTERS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T _A = 25°C			SN54ABT16646		SN74ABT16646		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V _{IK}		V _{CC} = 4.5 V, I _I = −18 mA		−1.2			−1.2		−1.2		V
V _{OH}		V _{CC} = 4.5 V, I _{OH} = −3 mA		2.5			2.5		2.5		V
		V _{CC} = 5 V, I _{OH} = −3 mA		3			3		3		
		V _{CC} = 4.5 V	I _{OH} = −24 mA	2			2				
			I _{OH} = −32 mA	2*					2		
V _{OL}		V _{CC} = 4.5 V		I _{OL} = 48 mA		0.55		0.55		V	
				I _{OL} = 64 mA		0.55*		0.55			
V _{hys}				100							mV
I _I	Control inputs	V _{CC} = 5.5 V, V _I = V _{CC} or GND		±1			±1		±1		μA
	A or B ports			±20			±20		±20		
I _{OZH} ‡		V _{CC} = 5.5 V, V _O = 2.7 V		10			10		10		μA
I _{OZL} ‡		V _{CC} = 5.5 V, V _O = 0.5 V		−10			−10		−10		μA
I _{off}		V _{CC} = 0, V _I or V _O ≤ 4.5 V		±100					±100		μA
I _{CEX}		V _{CC} = 5.5 V, V _O = 5.5 V	Outputs high	50			50		50		μA
I _O §		V _{CC} = 5.5 V, V _O = 2.5 V	−50 −100 −180	−50 −180			−50 −180		−50 −180		mA
I _{CC}	A or B ports	V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND	Outputs high	2			2		2		mA
			Outputs low	32			32		32		
			Outputs disabled	2			2		2		
ΔI _{CC} ¶	Data inputs	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND	Outputs enabled	50			50		50		μA
			Outputs disabled	50			50		50		
	Control inputs	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND	50			50		50			
C _i	Control inputs	V _I = 2.5 V or 0.5 V		4							pF
C _{io}	A or B ports	V _O = 2.5 V or 0.5 V		8							pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V_{CC} = 5 V.

‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 2)

		SN54ABT16646		UNIT		
		$V_{CC} = 5\text{ V},$ $T_A = 25^{\circ}\text{C}$			MIN	MAX
		MIN	MAX			
f_{clock}	Clock frequency	125		125	MHz	
t_w	Pulse duration, CLK high or low	4.3		4.3	ns	
t_{su}	Setup time, A or B before CLKAB \uparrow or CLKBA \uparrow	3.5		4	ns	
t_h	Hold time, A or B after CLKAB \uparrow or CLKBA \uparrow	0.5		0.5	ns	

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 2)

		SN74ABT16646		UNIT		
		$V_{CC} = 5\text{ V},$ $T_A = 25^{\circ}\text{C}$			MIN	MAX
		MIN	MAX			
f_{clock}	Clock frequency	125		125	MHz	
t_W	Pulse duration, CLK high or low	4.3		4.3	ns	
t_{su}	Setup time, A or B before CLKAB \uparrow or CLKBA \uparrow	3		3	ns	
t_h	Hold time, A or B after CLKAB \uparrow or CLKBA \uparrow	0		0	ns	

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16-BIT BUS TRANSCEIVERS AND REGISTERS

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABT16646					UNIT
			V _{CC} = 5 V, T _A = 25°C			MIN	MAX	
			MIN	TYP	MAX			
f _{max}			125			125		MHz
t _{PLH}	CLKBA or CLKAB	A or B	1.5	3.1	4	1	5	ns
t _{PHL}			1.5	3.2	4.1	1	5	
t _{PLH}	A or B	B or A	1	2.3	3.2	0.6	4	ns
t _{PHL}			1	3	4.1	0.6	4.9	
t _{PLH}	SAB or SBA†	B or A	1	2.9	4.3	0.6	5.3	ns
t _{PHL}			1	3.1	4.3	0.6	5.3	
t _{PZH}	\overline{OE}	A or B	1	3.4	4.6	0.6	5.9	ns
t _{PZL}			1.5	3.5	5.3	1	6	
t _{PHZ}	\overline{OE}	A or B	1.5	3.9	5.6	1	6.4	ns
t _{PLZ}			1.5	3.1	4.4	1	4.7	
t _{PZH}	DIR	A or B	1	3.2	4.5	0.6	5.8	ns
t _{PZL}			1.5	3.4	5.1	1	6.7	
t _{PHZ}	DIR	A or B	2	4.2	5.9	1.2	7.1	ns
t _{PLZ}			1.5	3.6	5.1	1	6.2	

† These parameters are measured with the internal output state of the storage register opposite that of the bus input.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74ABT16646					UNIT
			V _{CC} = 5 V, T _A = 25°C			MIN	MAX	
			MIN	TYP	MAX			
f _{max}			125			125		MHz
t _{PLH}	CLKBA or CLKAB	A or B	1.5	3.1	4	1.5	4.9	ns
t _{PHL}			1.5	3.2	4.1	1.5	4.7	
t _{PLH}	A or B	B or A	1	2.3	3.2	1	3.9	ns
t _{PHL}			1	3	4.1	1	4.6	
t _{PLH}	SAB or SBA†	B or A	1	2.9	4.3	1	5	ns
t _{PHL}			1	3.1	4.3	1	5	
t _{PZH}	\overline{OE}	A or B	1	3.4	4.6	1	5.5	ns
t _{PZL}			1.5	3.5	4.9	1.5	5.7	
t _{PHZ}	\overline{OE}	A or B	1.5	3.9	4.9	1.5	5.4	ns
t _{PLZ}			1.5	3.1	4.1	1.5	4.5	
t _{PZH}	DIR	A or B	1	3.2	4.5	1	5.4	ns
t _{PZL}			1.5	3.4	4.8	1.5	5.6	
t _{PHZ}	DIR	A or B	2	4.2	5.7	2	6.7	ns
t _{PLZ}			1.5	3.6	5.1	1.5	5.9	

† These parameters are measured with the internal output state of the storage register opposite that of the bus input.



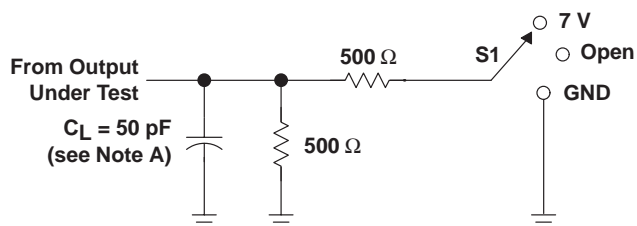
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16-BIT BUS TRANSCEIVERS AND REGISTERS

WITH 3-STATE OUTPUTS

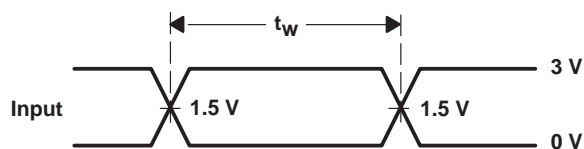
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PARAMETER MEASUREMENT INFORMATION

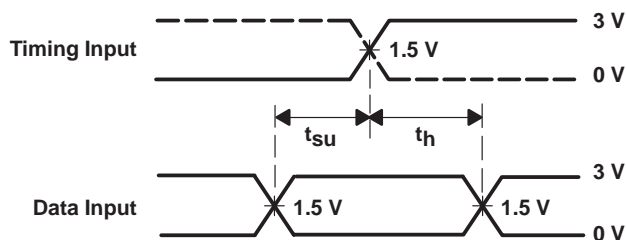


LOAD CIRCUIT

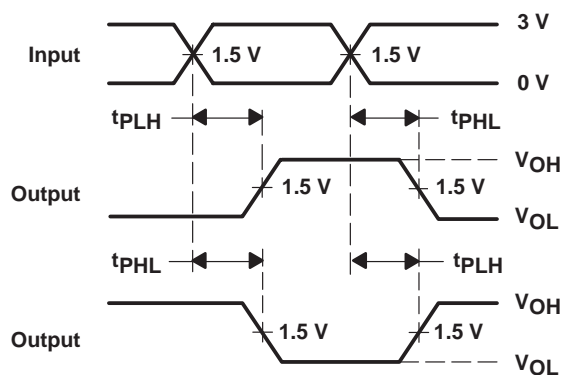
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



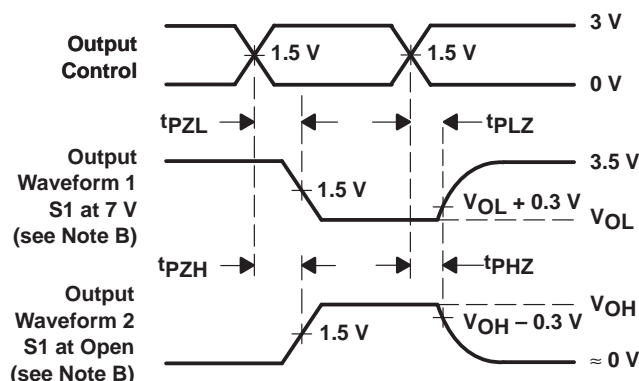
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-9450201QXA	ACTIVE	CFP	WD	56	1	TBD	Call TI	Level-NC-NC-NC
74ABT16646DGGRE4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT16646DGGR	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT16646DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT16646DLR	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT16646DLRG4	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54ABT16646WD	ACTIVE	CFP	WD	56	1	TBD	Call TI	Level-NC-NC-NC

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

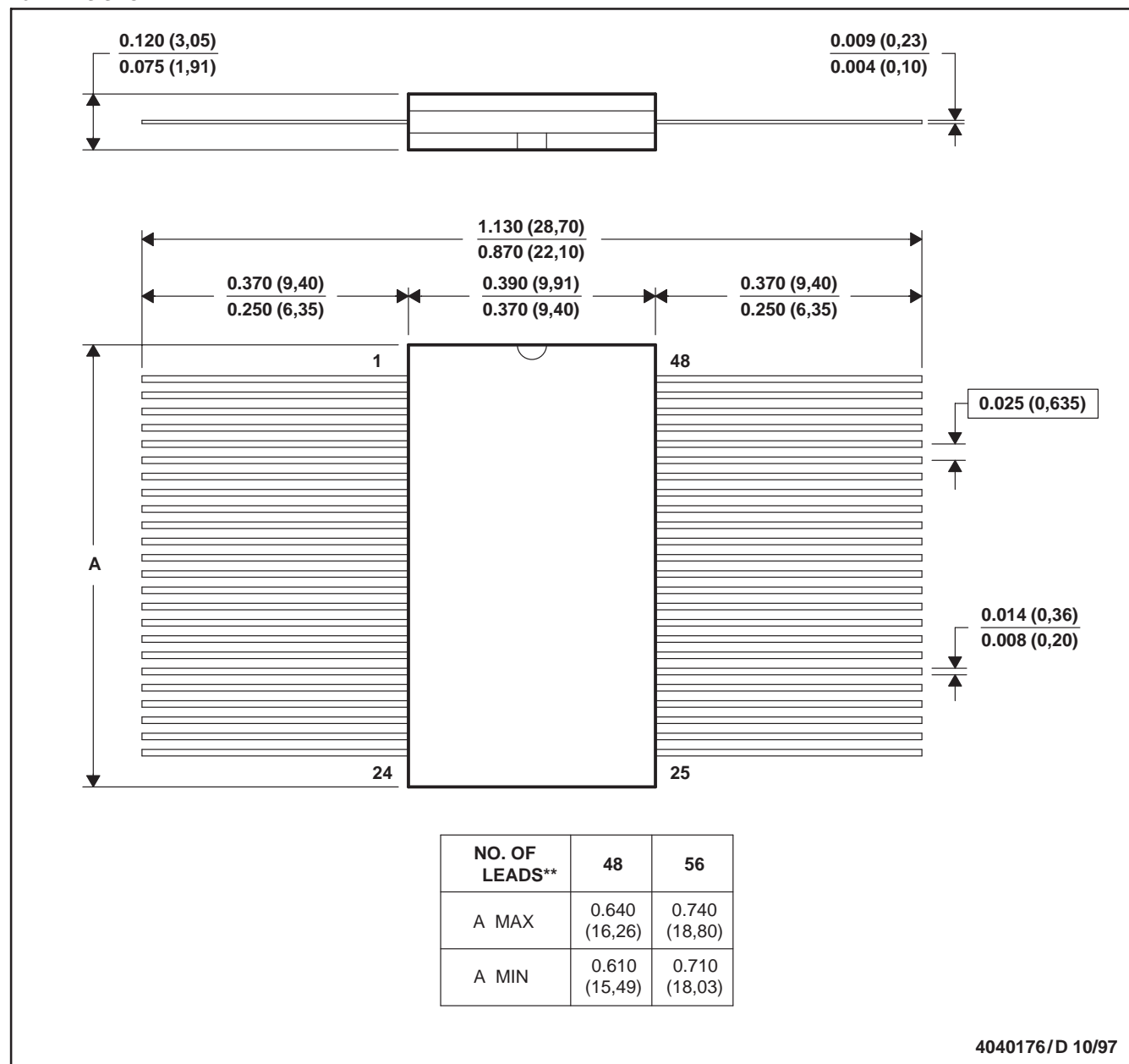
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WD (R-GDFP-F**)

CERAMIC DUAL FLATPACK

48 LEADS SHOWN

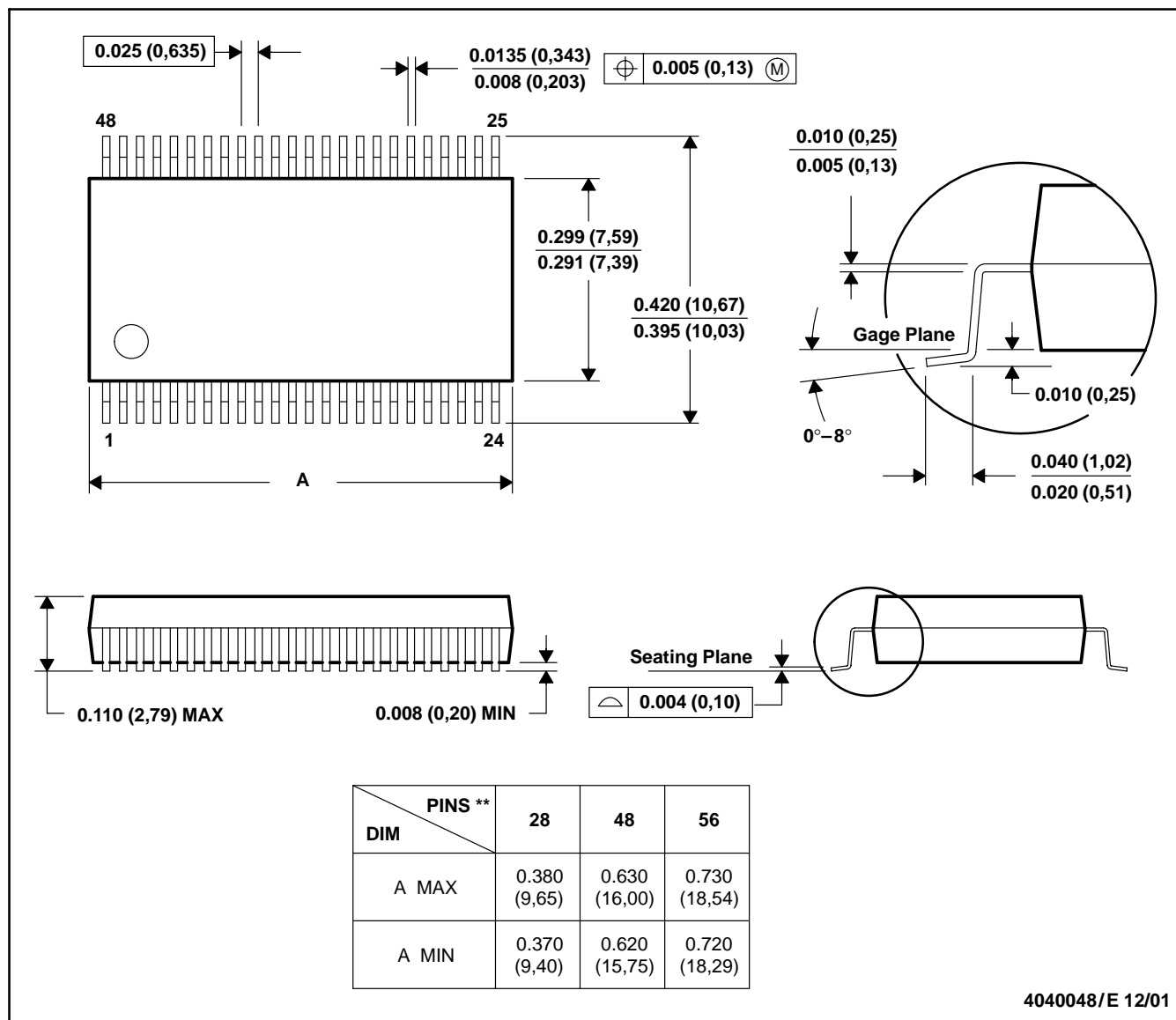


- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only.
 - Falls within MIL STD 1835: GDFP1-F48 and JEDEC MO-146AA
GDFP1-F56 and JEDEC MO-146AB

DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

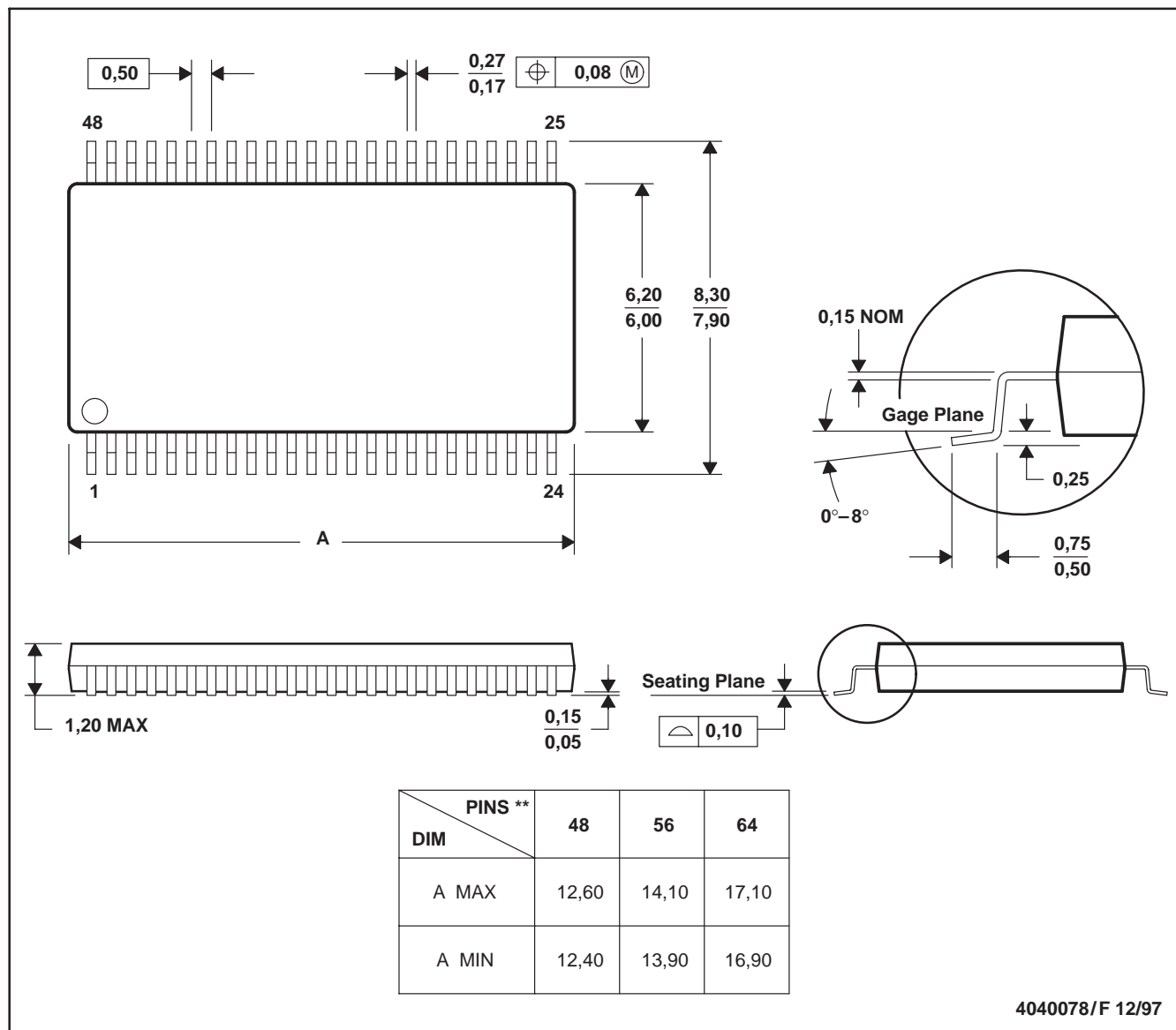


- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-118

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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