

ST33F1M

Smartcard MCU with 32-bit ARM® SecurCore® SC300™ CPU and 1.25 Mbytes high-density Flash memory

Data brief

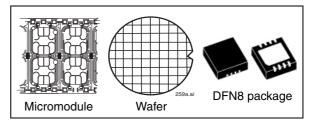
Features

ST33F1M major applications include:

- Mobile communications (GSM, 3G and CDMA)
- Java Card[™] applications
- Multimedia
- Mobile TV, banking & transportation

Hardware features

- ARM® SecurCore® SC300[™] 32-bit RISC core
- 30 Kbytes User RAM
- 1280 Kbytes User Flash memory with OTP area:
 - 10-year data retention
 - 100,000 Erase/Write cycles
 - Page granularity of 256 Bytes
 - Block granularity: 1 Kbyte
 - 256 Bytes of OTP for User
 - Page Erase time 5 ms
 - Block Erase 1 Kbyte in 15 ms
 - Programming performance up to 10μs/byte in Chained mode
 - Flash Erase / Write Protection software programmable on 128 Kbyte Sectors
- Asynchronous Receiver Transmitter supporting ISO/IEC 7816-3 T=0 and T=1 protocols
- Single Wire Protocol (SWP) Interface for communications with NFC router
- Optional Serial Peripheral Interface (SPI) Slave interface
- Two 16-bit timers with interrupt capability and one extra 16-bit timer with watchdog capability
- 1.8V, 3V and 5V supply voltage ranges
- External clock frequency from 1 up to 10 MHz
- High performance provided by:
 - CPU clock frequency up to 25 MHz
 - External clock multiplier (2x, 3x, and 4x)



- Current consumption compatible with GSM and ETSI specifications
- Power-saving Standby state
- Contact assignment compatible with ISO/IEC 7816-2
- ESD protection greater than 4 kV (HBM)
- 8-lead plastic small outline (208 mils body width) ECOPACK® package

Software features

- Secure Flash Loader
- Flash drivers

Security features

- Active shield
- Memory Protection Unit (MPU)
- Monitoring of environmental parameters
- Protection against faults
- ISO 3309 CRC calculation block
- True Random Number Generator
- Unique serial number on each die
- Hardware security-enhanced DES accelerator
- NESCRYPT coprocessor for public key cryptography algorithm

Development environment

Software development and firmware generation are supported by a comprehensive set of development tools dedicated to software design and validation:

- C Compiler
- Simulator
- Emulator

Description ST33F1M

1 Description

1.1 Hardware description

The ST33F1M is a serial access microcontroller designed for secure mobile applications that incorporates the most recent generation of ARM processors for embedded secure systems. Its SecurCore® SC300™ 32-bit RISC core is built on the Cortex™ M3 core with additional security features to help to protect against advanced forms of attacks.

Cadenced at 25MHz, the SC300[™] core brings great performance and excellent code density thanks to the Thumb®-2 instruction set.

The high-speed embedded Flash 1280 Kbyte memory introduces more flexibility to the system.

The ST33F1M also offers a serial communication interface fully compatible with the ISO/IEC 7816-3 standard (T=0, T=1) and a single-wire protocol (SWP) interface for communication with a near field communication (NFC) router in SIM/NFC applications.

An SPI Slave interface is also available for communication in non-SIM applications.

Three general purpose 16-bit timers are available; one configurable as a watchdog.

The ST33F1M features hardware accelerators for advanced cryptographic functions. The EDES peripheral provides a secure DES (Data Encryption Standard) algorithm implementation, while the NESCRYPT crypto-processor efficiently supports the public key algorithm.

The ST33F family operates in the -25 to +85°C temperature range and 1.8V, 3V and 5V supply voltage ranges. A comprehensive range of power-saving modes enables the design of efficient low-power applications.

In order to meet environmental requirements, ST (also) offers these devices in ECOPACK® packages. ECOPACK® packages are lead-free. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

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ST33F1M Description

SecurCore® Flash **EDES** RAM ST ROM NESCRYPT SC300™ memory Accelerator **CPU Core** NESCRYPT MPU ST ROM Firewall RAM Internal Bus (APB/AHB) True **IART** Clock Three **SWP** SPI Random Security CRC with Genewith 16-bit Admin-Number Slave Module RAM rator RAM timers (Optional) istrator Gene-Buffer Module Buffer rator CLK SWIO RESET Vcc GND 2 I/Os Ai15206_db

Figure 1. ST33F1M block diagram

1.2 Software development tools description

Dedicated SecurCore® SC300[™] software development tools are provided by ARM and Keil. This includes the Instruction Set Simulator (ISS) and C compiler. The documentation is available on the ARM and Keil web sites.

Moreover, STMicroelectronics provides:

- A time-accurate hardware emulator controlled by the Keil debugger and the ST development environment.
- A complete product simulator based on Keil's ISS simulator for the SecurCore® SC300™ CPU.
- A secured ROMed Flash Loader with very high-speed software downloading capabilities.

Revision history ST33F1M

2 Revision history

Table 1. Document revision history

Date	Revision	Changes
24-Jan-2011	1	Initial release.
28-Nov-2011	2	Updated Features and Description.

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