RICOH

0.8% LOW VOLTAGE DETECTOR WITH OUTPUT DELAY

NO.EA-161-120423

OUTLINE

The R3116x series are CMOS-based voltage detector ICs with high detector threshold accuracy and ultra-low supply current, which can be operated at an extremely low voltage and is used for system reset as an example.

Each of these ICs consists of a voltage reference unit, a comparator, resistors for detector threshold setting, an output driver, a hysteresis circuit and an output delay circuit. The detector threshold is internally fixed with high accuracy and does not require any adjustment.

Two output types, Nch open drain type and CMOS type are available.

The R3116x series are operable at a lower voltage than that of the R3112x series, and can be driven by a single battery.

Three types of packages, SOT-23-5, SC-82AB, and DFN(PLP)1010-4 are available.

FEATURES

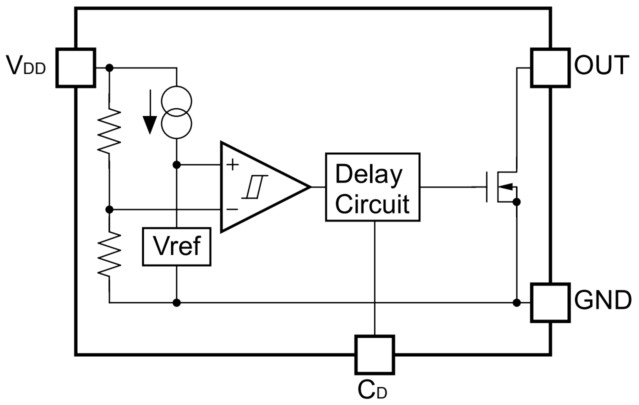
- Supply Current ....Typ. 0.35µA ($-V_{DET}$=1.5V, V_{DD}=$-V_{DET}$+1V)
- Operating Voltage Range...0.5V to 6.0V (T_{opt}=25°C)
- Detector Threshold Range..0.7V to 5.0V (0.1V steps)
  (For other voltages, please refer to MARK INFORMATIONS.)
- Detector Threshold Accuracy..±0.8% ($-V_{DET} \geq 1.5V$)
- Temperature-Drift Coefficient of Detector Threshold ....Typ. ±30ppm/°C
- Built-in Output Delay Circuit..Typ. 100ms with an external capacitor: 0.022µF
- Output Delay Time Accuracy..±15% ($-V_{DET} \geq 1.5V$)
- Output Types...Nch Open Drain "L" and CMOS
- Packages ....DFN(PLP)1010-4, SC-82AB, SOT-23-5

APPLICATIONS

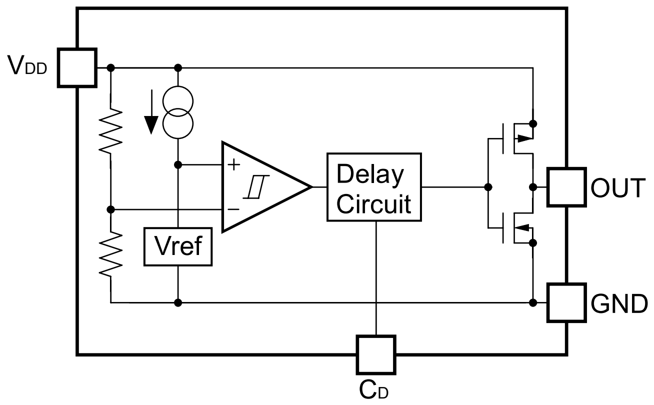
- CPU and Logic Circuit Reset
- Battery Checker
- Window Comparator
- Wave Shaping Circuit
- Battery Back-up Circuit
- Power Failure Detector

BLOCK DIAGRAMS

Nch Open Drain Output (R3116xxx1A)



CMOS Output (R3116xxx1C)



SELECTION GUIDE

The package type, the detector threshold, the output type and the taping type for the ICs can be selected at the users' request.

Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
R3116Kxx1∗-TR	DFN(PLP)1010-4	10,000 pcs	Yes	Yes
R3116Qxx1∗-TR-FE	SC-82AB	3,000 pcs	Yes	Yes
R3116Nxx1∗-TR-FE	SOT-23-5	3,000 pcs	Yes	Yes

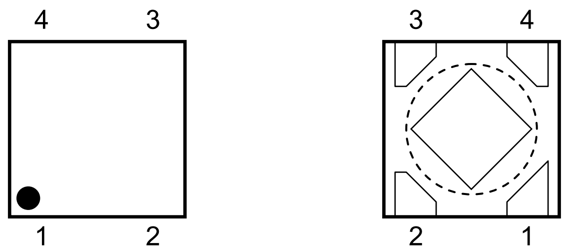
xx: The detector threshold can be designated in the range from 0.7V(07) to 5.0V(50) in 0.1V steps.
(For other voltages, please refer to MARK INFORMATIONS.)

∗ : Designation of Output Type
(A) Nch Open Drain
(C) CMOS

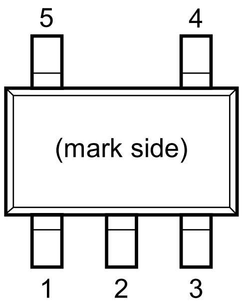
PIN CONFIGURATIONS

● **DFN(PLP)1010-4***

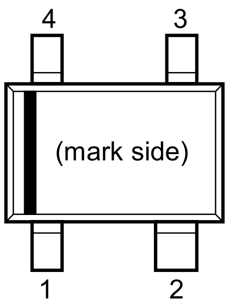
Top View **Bottom View**



● **SOT-23-5**



● **SC-82AB**



PIN DESCRIPTIONS

● DFN(PLP)1010-4*

Pin No.	Symbol	Description
1	OUT	Output Pin ("L" at detection)
2	C_D	Pin for External Capacitor (for setting output delay)
3	GND	Ground Pin
4	V_{DD}	Input Pin

*) Tab is GND level. (They are connected to the reverse side of this IC.)
The tab is better to be connected to the GND, but leaving it open is also acceptable.

● SOT-23-5

Pin No.	Symbol	Description
1	OUT	Output Pin ("L" at detection)
2	V_{DD}	Input Pin
3	GND	Ground Pin
4	NC	No Connection
5	C_D	Pin for External Capacitor (for setting output delay)

● SC-82AB

Pin No.	Symbol	Description
1	V_{DD}	Input Pin
2	GND	Ground Pin
3	C_D	Pin for External Capacitor (for setting output delay)
4	OUT	Output Pin ("L" at detection)

ABSOLUTE MAXIMUM RATINGS

Symbol	Item	Rating	Unit
V_{DD}	Supply Voltage	7.0	V
V_{OUT}	Output Voltage (Nch Open Drain Output)	V_{SS}–0.3 to 7.0	V
	Output Voltage (CMOS Output)	V_{SS}–0.3 to V_{DD}+0.3	
I_{OUT}	Output Current	20	mA
P_D	Power Dissipation (SOT-23-5)*	420	mW
	Power Dissipation (SC-82AB)*	380	
	Power Dissipation (DFN(PLP)1010-4)*	400	
Topt	Operating Temperature Range	–40 to 85	°C
Tstg	Storage Temperature Range	–55 to 125	°C

*) For Power Dissipation, please refer to PACKAGE INFORMATION.

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause the permanent damages and may degrade the life time and safety for both device and system using the device in the field.
The functional operation at or over these absolute maximum ratings is not assured.

RECOMMENDED OPERATING CONDITIONS (ELECTRICAL CHARACTERISTICS)

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if when they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

ELECTRICAL CHARACTERISTICS

- **R3116xxx1A/C** ☐ values indicate $-40°C \leq Topt \leq 85°C$, unless otherwise noted. Topt=25°C

Symbol	Item	Conditions			Min.	Typ.	Max.	Unit
$-V_{DET}$	Detector Threshold	Topt=25°C	$1.5V < -V_{DET} \leq 5.0V$		$-V_{DET} \times 0.992$		$-V_{DET} \times 1.008$	V
			$0.7V \leq -V_{DET} \leq 1.5V$		-12		+12	mV
		$-40°C \leq Topt \leq 85°C$	$1.5V < -V_{DET} \leq 5.0V$		$-V_{DET} \times 0.985$		$-V_{DET} \times 1.015$	V
			$0.7V \leq -V_{DET} \leq 1.5V$		-22.5		+22.5	mV
V_{HYS}	Detector Threshold Hysteresis				$-V_{DET} \times 0.04$		$-V_{DET} \times 0.07$	V
I_{SS}	Supply Current	$V_{DD}=-V_{DET} -0.1V$	$0.7V \leq -V_{DET} < 1.6V$				1.40	µA
			$1.6V \leq -V_{DET} < 3.1V$				1.50	
			$3.1V \leq -V_{DET} < 4.1V$				1.60	
			$4.1V \leq -V_{DET} \leq 5.0V$				1.70	
		$V_{DD}=-V_{DET} +0.1V$	$0.7V \leq -V_{DET} < 1.6V$				1.20	
			$1.6V \leq -V_{DET} < 3.1V$				1.20	
			$3.1V \leq -V_{DET} < 4.1V$				1.30	
			$4.1V \leq -V_{DET} \leq 5.0V$				1.40	
V_{DDH}	Maximum Operating Voltage						6	V
V_{DDL}	Minimum Operating Voltage*1	Topt=25°C					0.50	V
		$-40°C \leq Topt \leq 85°C$					0.55	
I_{OUT}	Output Current (Driver Output Pin)	Nch	$V_{DD}=0.55V, V_{DS}=0.05V$		7			µA
			$0.7V \leq -V_{DET} < 1.1V$	$V_{DD}=0.6V, V_{DS}=0.5V$	0.02			mA
			$1.1V \leq -V_{DET} < 1.6V$	$V_{DD}=1.0V, V_{DS}=0.5V$	0.40			
			$1.6V \leq -V_{DET} < 3.1V$	$V_{DD}=1.5V, V_{DS}=0.5V$	1.00			
			$3.1V \leq -V_{DET} \leq 5.0V$	$V_{DD}=3.0V, V_{DS}=0.5V$	2.40			
		Pch*2	$0.7V \leq -V_{DET} < 4.0V$	$V_{DD}=4.5V, V_{DS}=-2.1V$	0.65			mA
			$4.0V \leq -V_{DET} \leq 5.0V$	$V_{DD}=6.0V, V_{DS}=-2.1V$	0.90			
I_{LEAK}	Nch Driver Leakage Current*3	$V_{DD}=6.0V, V_{DS}=7.0V$					80	nA
$\Delta -V_{DET}/\Delta Topt$	Detector Threshold Temperature Coefficient					±30		ppm/°C
t_D	Output Delay Time	$C_D=0.022µF$, $V_{DD}=-V_{DET}-0.1V$ to $-V_{DET} \times 1.1V$	Topt=25°C, $0.7V \leq -V_{DET} < 1.5V$		80	100	130	ms
			Topt=25°C, $1.5V \leq -V_{DET} \leq 5.0V$		85		115	
			$-40°C \leq Topt \leq 85°C$, $0.7V \leq -V_{DET} < 1.5V$		70	100	150	
			$-40°C \leq Topt \leq 85°C$, $1.5V \leq -V_{DET} \leq 5.0V$		75		135	

All of unit are tested and specified under load conditions such that Topt=25°C except for Detector Threshold Temperature Coefficient.

*1: Minimum operating voltage means the value of input voltage when output voltage maintains 0.1V or less.
(In case of Nch Open Drain Output type, the output pin is pulled up with a resistance of 470kΩ to 5.0V)

*2: In case of CMOS type

*3: In case of Nch Open Drain type

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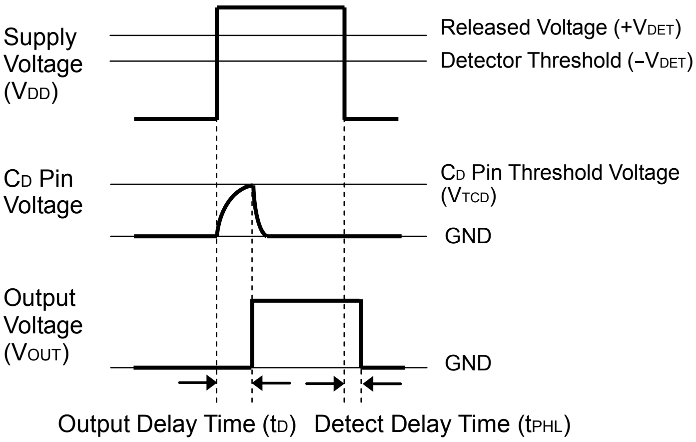
TIMING CHART



When the supply voltage, which is higher than released voltage, is forced to V_{DD} pin, charge to an external capacitor starts, then C_D pin voltage increases. Until the C_D pin voltage reaches to C_D pin threshold voltage, output voltage maintains "L". When the C_D pin voltage becomes higher than C_D pin threshold voltage, output voltage is reversed from "L" to "H". Where the time interval between the rising edge of supply voltage and output voltage reverse point means output delay time.

When the output voltage reverses from "L" to "H", the external capacitor starts to discharge. Therefore, when lower voltage than the detector threshold voltage is forced to V_{DD} pin, the output voltage reverses from "H" to "L" thus the detect delay time is constant not being affected by the external capacitor.

- **Output Delay Time**

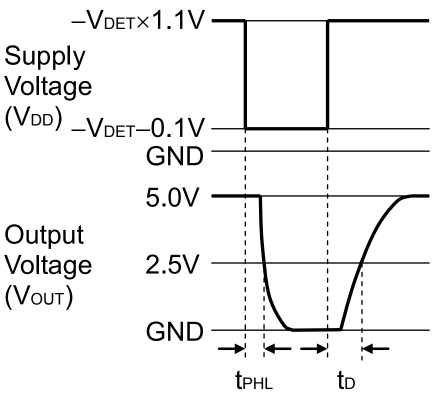
Output Delay Time (t_D) can be calculated with the next formula using the external capacitor:

$t_D(s) = 4.5 \times 10^6 \times C_D(F)$

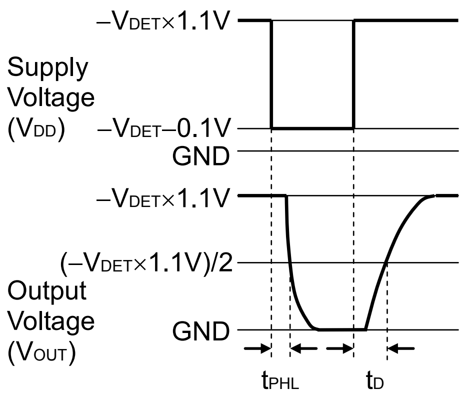
DEFINITION OF OUTPUT DELAY TIME

Output Delay Time (t_D) is defined as follows:

1. In the case of Nch Open Drain Output:
   Under the condition of the output pin (OUT) is pulled up through a resistor of 470kΩ to 5V, the time interval between the rising edge of V_{DD} pulse from (-V_{DET})–0.1V to (-V_{DET})×1.1V pulse voltage is supplied, the becoming of the output voltage to 2.5V.
2. In the case of CMOS Output:
   The time interval between the rising edge of V_{DD} pulse from (-V_{DET})–0.1V to (-V_{DET})×1.1V pulse voltage is supplied, the becoming of the output voltage to ((-V_{DET})×1.1V)/2.



Nch Open Drain Output
(R3116xxx1A)



CMOS Output
(R3116xxx1C)

RICOH

ELECTRICAL CHARACTERISTICS BY DETECTOR THRESHOLD

• R3116x071A/C to R3116x501A/C

Bold values are checked and guaranteed by design engineering at –40°C ≤ Topt ≤ 85°C, unless otherwise noted.

Topt=25°C

Part Number	Detector Threshold1		Detector Threshold2		Detector Threshold Hysteresis		Supply Current1		Supply Current2		Max. Op. Voltage	Min. Op. Voltage
	-VDET1 [V]		-VDET2 [V]		VHYS [V]		ISS1 [μA]		ISS2 [μA]		VDDH [V]	VDDL [V]
	Min.	Max.	Min.	Max.	Min.	Max.	Cond.	Max.	Cond.	Max.	Max.	Max.
R3116x071A/C	0.6880	0.7120	**0.6775**	**0.7225**	**0.028**	**0.049**	VDD= -VDET -0.1V	**1.400**	VDD= -VDET +1.0V	**1.200**	**6**	0.50 / **0.55** *Note1
R3116x081A/C	0.7880	0.8120	**0.7775**	**0.8225**	**0.032**	**0.056**	VDD= -VDET -0.1V	**1.400**	VDD= -VDET +1.0V	**1.200**	**6**	0.50 / **0.55** *Note1
R3116x091A/C	0.8880	0.9120	**0.8775**	**0.9225**	**0.036**	**0.063**	VDD= -VDET -0.1V	**1.400**	VDD= -VDET +1.0V	**1.200**	**6**	0.50 / **0.55** *Note1
R3116x101A/C	0.9880	1.0120	**0.9775**	**1.0225**	**0.040**	**0.070**	VDD= -VDET -0.1V	**1.400**	VDD= -VDET +1.0V	**1.200**	**6**	0.50 / **0.55** *Note1
R3116x111A/C	1.0880	1.1120	**1.0775**	**1.1225**	**0.044**	**0.077**	VDD= -VDET -0.1V	**1.400**	VDD= -VDET +1.0V	**1.200**	**6**	0.50 / **0.55** *Note1
R3116x121A/C	1.1880	1.2120	**1.1775**	**1.2225**	**0.048**	**0.084**	VDD= -VDET -0.1V	**1.400**	VDD= -VDET +1.0V	**1.200**	**6**	0.50 / **0.55** *Note1
R3116x131A/C	1.2880	1.3120	**1.2775**	**1.3225**	**0.052**	**0.091**	VDD= -VDET -0.1V	**1.400**	VDD= -VDET +1.0V	**1.200**	**6**	0.50 / **0.55** *Note1
R3116x141A/C	1.3880	1.4120	**1.3775**	**1.4225**	**0.056**	**0.098**	VDD= -VDET -0.1V	**1.400**	VDD= -VDET +1.0V	**1.200**	**6**	0.50 / **0.55** *Note1
R3116x151A/C	1.4880	1.5120	**1.4775**	**1.5225**	**0.060**	**0.105**	VDD= -VDET -0.1V	**1.400**	VDD= -VDET +1.0V	**1.200**	**6**	0.50 / **0.55** *Note1
R3116x161A/C	1.5872	1.6128	**1.5760**	**1.6240**	**0.064**	**0.112**	VDD= -VDET -0.1V	**1.500**	VDD= -VDET +1.0V	**1.200**	**6**	0.50 / **0.55** *Note1
R3116x171A/C	1.6864	1.7136	**1.6745**	**1.7255**	**0.068**	**0.119**	VDD= -VDET -0.1V	**1.500**	VDD= -VDET +1.0V	**1.200**	**6**	0.50 / **0.55** *Note1
R3116x181A/C	1.7856	1.8144	**1.7730**	**1.8270**	**0.072**	**0.126**	VDD= -VDET -0.1V	**1.500**	VDD= -VDET +1.0V	**1.200**	**6**	0.50 / **0.55** *Note1
R3116x191A/C	1.8848	1.9152	**1.8715**	**1.9285**	**0.076**	**0.133**	VDD= -VDET -0.1V	**1.500**	VDD= -VDET +1.0V	**1.200**	**6**	0.50 / **0.55** *Note1
R3116x201A/C	1.9840	2.0160	**1.9700**	**2.0300**	**0.080**	**0.140**	VDD= -VDET -0.1V	**1.500**	VDD= -VDET +1.0V	**1.200**	**6**	0.50 / **0.55** *Note1
R3116x211A/C	2.0832	2.1168	**2.0685**	**2.1315**	**0.084**	**0.147**	VDD= -VDET -0.1V	**1.500**	VDD= -VDET +1.0V	**1.200**	**6**	0.50 / **0.55** *Note1
R3116x221A/C	2.1824	2.2176	**2.1670**	**2.2330**	**0.088**	**0.154**	VDD= -VDET -0.1V	**1.500**	VDD= -VDET +1.0V	**1.200**	**6**	0.50 / **0.55** *Note1
R3116x231A/C	2.2816	2.3184	**2.2655**	**2.3345**	**0.092**	**0.161**	VDD= -VDET -0.1V	**1.500**	VDD= -VDET +1.0V	**1.200**	**6**	0.50 / **0.55** *Note1
R3116x241A/C	2.3808	2.4192	**2.3640**	**2.4360**	**0.096**	**0.168**	VDD= -VDET -0.1V	**1.500**	VDD= -VDET +1.0V	**1.200**	**6**	0.50 / **0.55** *Note1
R3116x251A/C	2.4800	2.5200	**2.4625**	**2.5375**	**0.100**	**0.175**	VDD= -VDET -0.1V	**1.500**	VDD= -VDET +1.0V	**1.200**	**6**	0.50 / **0.55** *Note1
R3116x261A/C	2.5792	2.6208	**2.5610**	**2.6390**	**0.104**	**0.182**	VDD= -VDET -0.1V	**1.500**	VDD= -VDET +1.0V	**1.200**	**6**	0.50 / **0.55** *Note1
R3116x271A/C	2.6784	2.7216	**2.6595**	**2.7405**	**0.108**	**0.189**	VDD= -VDET -0.1V	**1.500**	VDD= -VDET +1.0V	**1.200**	**6**	0.50 / **0.55** *Note1
R3116x281A/C	2.7776	2.8224	**2.7580**	**2.8420**	**0.112**	**0.196**	VDD= -VDET -0.1V	**1.500**	VDD= -VDET +1.0V	**1.200**	**6**	0.50 / **0.55** *Note1
R3116x291A/C	2.8768	2.9232	**2.8565**	**2.9435**	**0.116**	**0.203**	VDD= -VDET -0.1V	**1.500**	VDD= -VDET +1.0V	**1.200**	**6**	0.50 / **0.55** *Note1
R3116x301A/C	2.9760	3.0240	**2.9550**	**3.0450**	**0.120**	**0.210**	VDD= -VDET -0.1V	**1.500**	VDD= -VDET +1.0V	**1.200**	**6**	0.50 / **0.55** *Note1
R3116x311A/C	3.0752	3.1248	**3.0535**	**3.1465**	**0.124**	**0.217**	VDD= -VDET -0.1V	**1.600**	VDD= -VDET +1.0V	**1.300**	**6**	0.50 / **0.55** *Note1
R3116x321A/C	3.1744	3.2256	**3.1520**	**3.2480**	**0.128**	**0.224**	VDD= -VDET -0.1V	**1.600**	VDD= -VDET +1.0V	**1.300**	**6**	0.50 / **0.55** *Note1
R3116x331A/C	3.2736	3.3264	**3.2505**	**3.3495**	**0.132**	**0.231**	VDD= -VDET -0.1V	**1.600**	VDD= -VDET +1.0V	**1.300**	**6**	0.50 / **0.55** *Note1
R3116x341A/C	3.3728	3.4272	**3.3490**	**3.4510**	**0.136**	**0.238**	VDD= -VDET -0.1V	**1.600**	VDD= -VDET +1.0V	**1.300**	**6**	0.50 / **0.55** *Note1
R3116x351A/C	3.4720	3.5280	**3.4475**	**3.5525**	**0.140**	**0.245**	VDD= -VDET -0.1V	**1.600**	VDD= -VDET +1.0V	**1.300**	**6**	0.50 / **0.55** *Note1
R3116x361A/C	3.5712	3.6288	**3.5460**	**3.6540**	**0.144**	**0.252**	VDD= -VDET -0.1V	**1.600**	VDD= -VDET +1.0V	**1.300**	**6**	0.50 / **0.55** *Note1
R3116x371A/C	3.6704	3.7296	**3.6445**	**3.7555**	**0.148**	**0.259**	VDD= -VDET -0.1V	**1.600**	VDD= -VDET +1.0V	**1.300**	**6**	0.50 / **0.55** *Note1
R3116x381A/C	3.7696	3.8304	**3.7430**	**3.8570**	**0.152**	**0.266**	VDD= -VDET -0.1V	**1.600**	VDD= -VDET +1.0V	**1.300**	**6**	0.50 / **0.55** *Note1
R3116x391A/C	3.8688	3.9312	**3.8415**	**3.9585**	**0.156**	**0.273**	VDD= -VDET -0.1V	**1.600**	VDD= -VDET +1.0V	**1.300**	**6**	0.50 / **0.55** *Note1
R3116x401A/C	3.9680	4.0320	**3.9400**	**4.0600**	**0.160**	**0.280**	VDD= -VDET -0.1V	**1.600**	VDD= -VDET +1.0V	**1.300**	**6**	0.50 / **0.55** *Note1
R3116x411A/C	4.0672	4.1328	**4.0385**	**4.1615**	**0.164**	**0.287**	VDD= -VDET -0.1V	**1.700**	VDD= -VDET +1.0V	**1.400**	**6**	0.50 / **0.55** *Note1
R3116x421A/C	4.1664	4.2336	**4.1370**	**4.2630**	**0.168**	**0.294**	VDD= -VDET -0.1V	**1.700**	VDD= -VDET +1.0V	**1.400**	**6**	0.50 / **0.55** *Note1
R3116x431A/C	4.2656	4.3344	**4.2355**	**4.3645**	**0.172**	**0.301**	VDD= -VDET -0.1V	**1.700**	VDD= -VDET +1.0V	**1.400**	**6**	0.50 / **0.55** *Note1
R3116x441A/C	4.3648	4.4352	**4.3340**	**4.4660**	**0.176**	**0.308**	VDD= -VDET -0.1V	**1.700**	VDD= -VDET +1.0V	**1.400**	**6**	0.50 / **0.55** *Note1
R3116x451A/C	4.4640	4.5360	**4.4325**	**4.5675**	**0.180**	**0.315**	VDD= -VDET -0.1V	**1.700**	VDD= -VDET +1.0V	**1.400**	**6**	0.50 / **0.55** *Note1
R3116x461A/C	4.5632	4.6368	**4.5310**	**4.6690**	**0.184**	**0.322**	VDD= -VDET -0.1V	**1.700**	VDD= -VDET +1.0V	**1.400**	**6**	0.50 / **0.55** *Note1
R3116x471A/C	4.6624	4.7376	**4.6295**	**4.7705**	**0.188**	**0.329**	VDD= -VDET -0.1V	**1.700**	VDD= -VDET +1.0V	**1.400**	**6**	0.50 / **0.55** *Note1
R3116x481A/C	4.7616	4.8384	**4.7280**	**4.8720**	**0.192**	**0.336**	VDD= -VDET -0.1V	**1.700**	VDD= -VDET +1.0V	**1.400**	**6**	0.50 / **0.55** *Note1
R3116x491A/C	4.8608	4.9392	**4.8265**	**4.9735**	**0.196**	**0.343**	VDD= -VDET -0.1V	**1.700**	VDD= -VDET +1.0V	**1.400**	**6**	0.50 / **0.55** *Note1
R3116x501A/C	4.9600	5.0400	**4.9250**	**5.0750**	**0.200**	**0.350**	VDD= -VDET -0.1V	**1.700**	VDD= -VDET +1.0V	**1.400**	**6**	0.50 / **0.55** *Note1

*Note1) VDD value when output voltage is equal or less than 0.1V. In the case of Nch Open Drain output type, the output pin is pulled up to 5.0V through 470kΩ resistor.

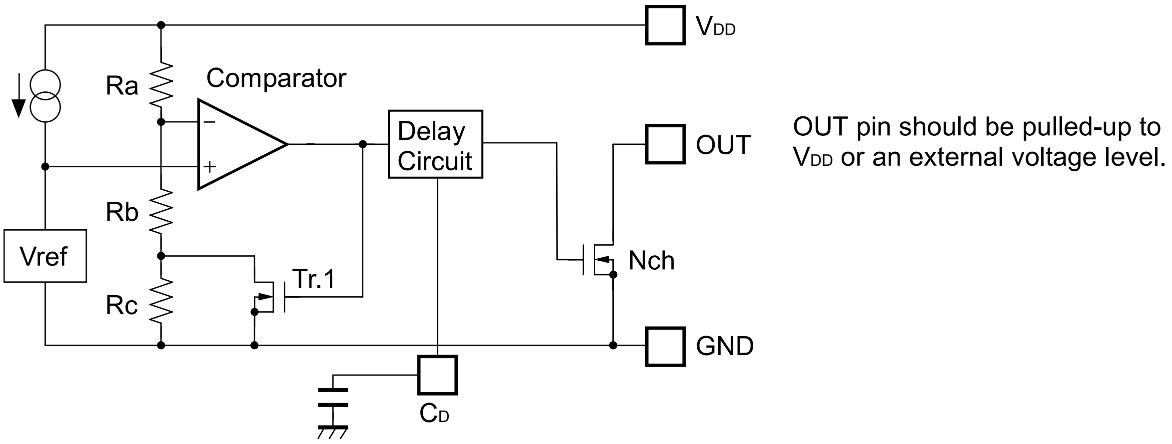
Nch Driver Output Current1		Nch Driver Output Current2		Pch Driver Output Current		Nch Driver Leakage Current		Detector Threshold Temperature Coefficient	Output Delay Time		
I_{OUT1} [μA]		I_{OUT2} [mA]		I_{OUT3} [mA]		I_{LEAK} [nA]		Δ-V_{DET}/ΔT_{opt} [ppm/°C]	t_D [ms]		
Cond.	Min.	Cond.	Min.	Cond.	Min.	Cond.	Max.	Typ.	Cond.	Min.	Max.
V_{DD}=0.55V V_{DS}=0.05V	7	V_{DD}=0.6V V_{DS}=0.5V	0.020	V_{DD}=4.5V V_{DS}=-2.1V	0.650	V_{DD}=6.0V V_{DS}=7.0V	80	±30	V_{DD}=-V_{DET}-0.1V ↓ -V_{DET}×1.1V *Note2	80 70	130 150
		V_{DD}=1.0V V_{DS}=0.5V	0.400								
		V_{DD}=1.5V V_{DS}=0.5V	1.000							85 75	115 135
		V_{DD}=3.0V V_{DS}=0.5V	2.400	V_{DD}=6.0V V_{DS}=-2.1V	0.900						

*Note2) 1. In the case of CMOS output type:
When the voltage is forced from (-V_{DET})–0.1V to (-V_{DET})×1.1V pulse voltage is added to V_{DD}, time interval that the output voltage reaches ((-V_{DET})×1.1V)/2.

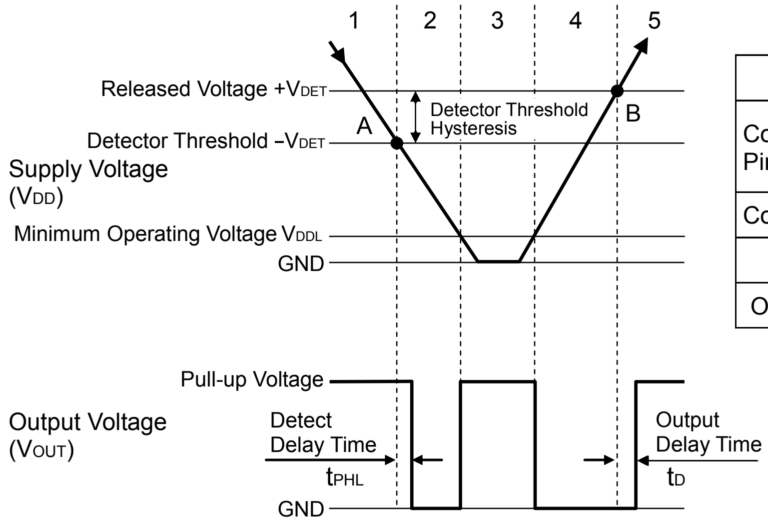
2. In the case of Nch Open Drain output type:
The output pin is pulled up to 5.0V through 470kΩ, and when the voltage is forced from (-V_{DET})–0.1V to (-V_{DET})×1.1V pulse voltage is added to V_{DD}, time interval that the output voltage reaches 2.5V.

OPERATION

• Operation of R3116xxx1A



Block Diagram (R3116xxx1A)



Step		1	2	3	4	5
Comparator (−) Pin Input Voltage		I	II	II	II	I
Comparator Output		L	H	Indefinite	H	L
Tr.1		OFF	ON	Indefinite	ON	OFF
Output Tr.	Nch	OFF	ON	Indefinite	ON	OFF

I $\frac{Rb+Rc}{Ra+Rb+Rc} \times V_{DD}$

II $\frac{Rb}{Ra+Rb} \times V_{DD}$

Operation Diagram

• Explanation of operation

Step 1. The output voltage is equal to the pull-up voltage.

Step 2. At Point "A", Vref ≧ V_{DD}×(Rb+Rc)/(Ra+Rb+Rc) is true, as a result, the output of comparator is reversed from "L" to "H", therefore the output voltage becomes the GND level. The voltage level of Point A means a detector threshold voltage ($-V_{DET}$).

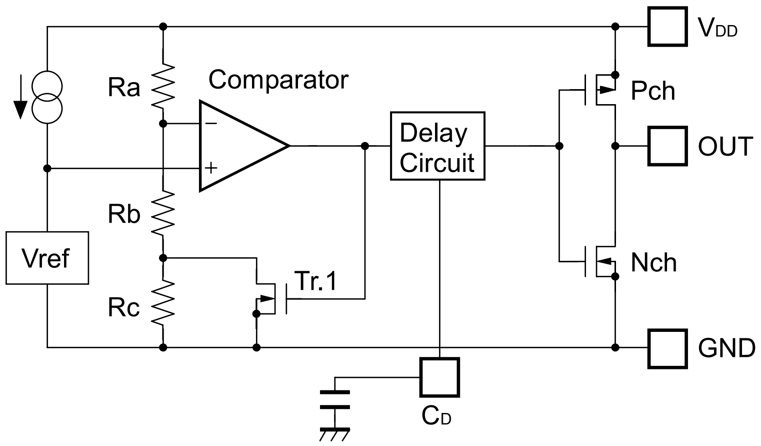
Step 3. When the supply voltage is lower than the minimum operating voltage, the operation of the output transistor becomes indefinite. The output voltage is equal to the pull-up voltage.

Step 4. The output voltage is equal to the GND level.

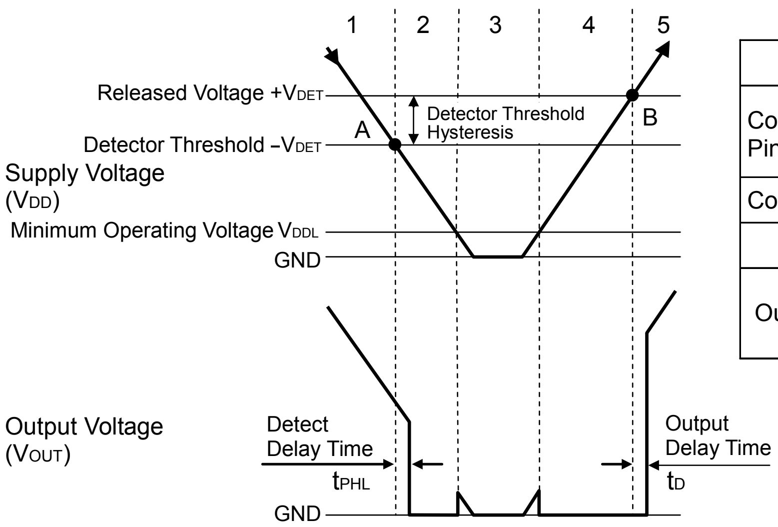
Step 5. At Point "B", Vref ≦ V_{DD}×Rb/(Ra+Rb) is true, as a result, the output of comparator is reversed from "H" to "L", then the output voltage is equal to the pull-up voltage. The voltage level of Point B means a released voltage ($+V_{DET}$).

∗) The difference between a released voltage and a detector threshold voltage is a detector threshold hysteresis.

• Operation of R3116xxx1C



Block Diagram (R3116xxx1C)



Step		1	2	3	4	5
Comparator (–) Pin Input Voltage		I	II	II	II	I
Comparator Output		L	H	Indefinite	H	L
Tr.1		OFF	ON	Indefinite	ON	OFF
Output Tr.	Pch	ON	OFF	Indefinite	OFF	ON
	Nch	OFF	ON	Indefinite	ON	OFF

I $\dfrac{Rb+Rc}{Ra+Rb+Rc} \times V_{DD}$

II $\dfrac{Rb}{Ra+Rb} \times V_{DD}$

Operation Diagram

• Explanation of operation

Step 1. The output voltage is equal to the supply voltage (V_{DD}).

Step 2. At Point "A", Vref $\geqq V_{DD} \times (Rb+Rc)/(Ra+Rb+Rc)$ is true, as a result, the output of comparator is reversed from "L" to "H", therefore the output voltage becomes the GND level. The voltage level of Point A means a detector threshold voltage ($-V_{DET}$).

Step 3. When the supply voltage is lower than the minimum operating voltage, the operation of the output transistor becomes indefinite.

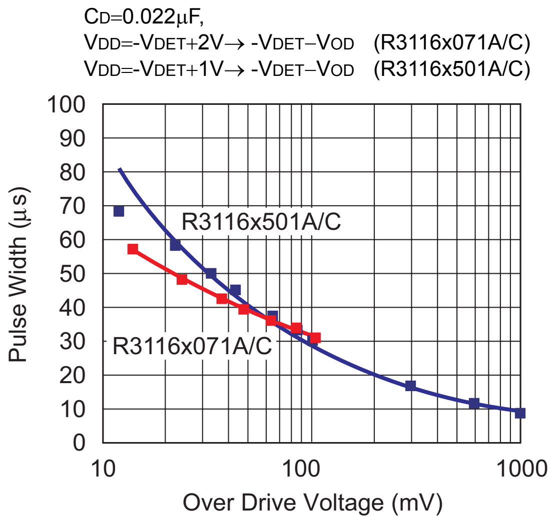
Step 4. The output voltage is equal to the GND level.

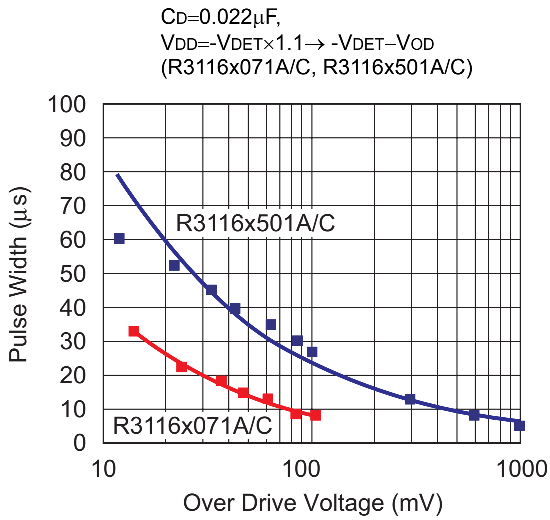
Step 5. At Point "B", Vref $\leqq V_{DD} \times Rb/(Ra+Rb)$ is true, as a result, the output of comparator is reversed from "H" to "L", then the output voltage is equal to the supply voltage (V_{DD}). The voltage level of Point B means a released voltage ($+V_{DET}$).

∗) The difference between a released voltage and a detector threshold voltage is a detector threshold hysteresis.

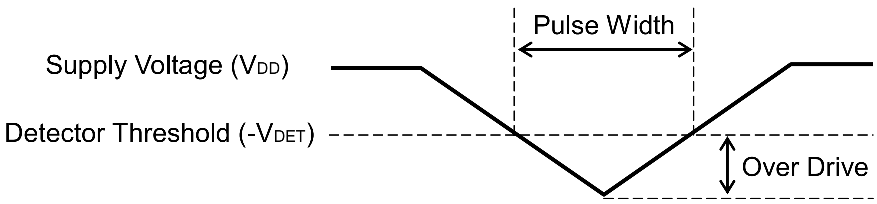
Detector Operation vs. glitch input voltage to the VDD pin

When the R3116x is at released, if the pulse voltage which the detector threshold or lower voltage, the graph below means that the relation between pulse width and the amplitude of the swing to keep the released state for the R3116x.





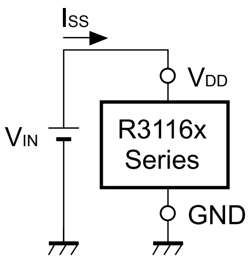
∗VOD: Over Drive Voltage



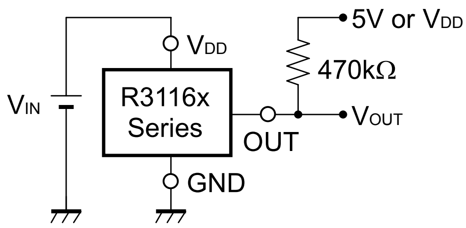
VDD Input Waveform

This graph shows the maximum pulse conditions to keep the released voltage. If the pulse with larger amplitude or wider width than the graph above, is input to VDD pin, the reset signal may be output.

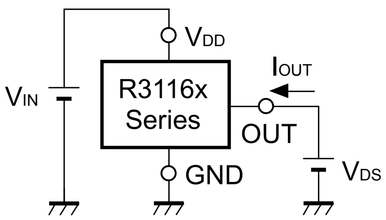
TEST CIRCUITS



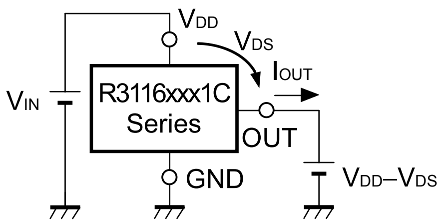
Supply Current Test Circuit



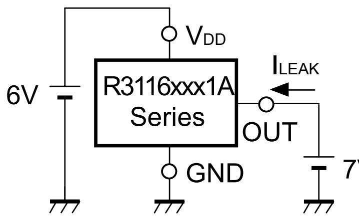
Detector Threshold Test Circuit
(Pull-up circuit is not necessary for CMOS Output type.)



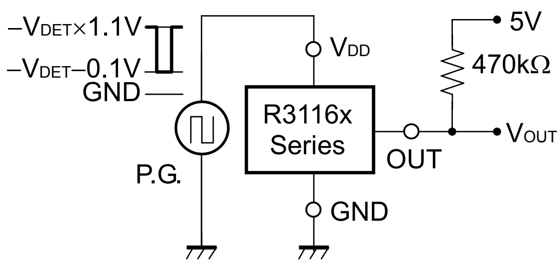
Nch Driver Output Current Test Circuit



Pch Driver Output Current Test Circuit
∗Apply to CMOS Output type only



Nch Driver Leakage Current Test Circuit
∗Apply to Nch Driver Output type only

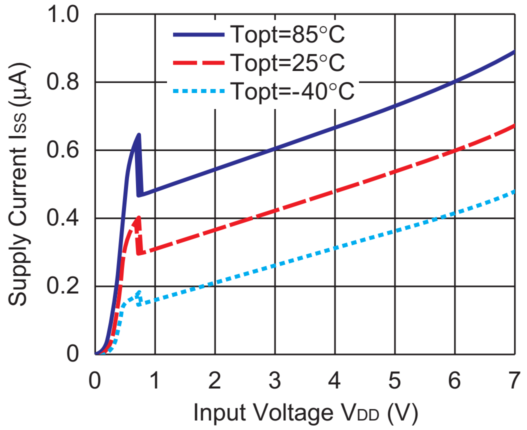


Output Delay Time Test Circuit
(Pull-up circuit is not necessary for CMOS Output type.)

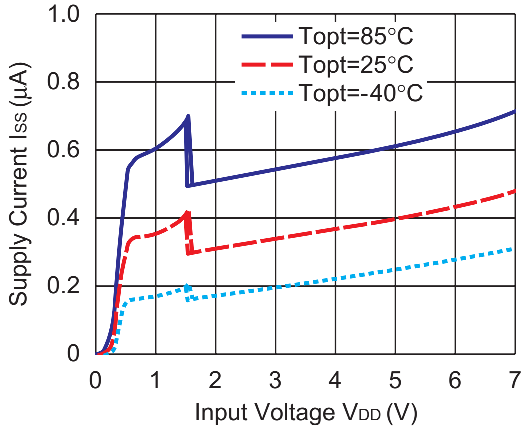
TYPICAL CHARACTERISTICS

1) Supply Current vs. Input Voltage

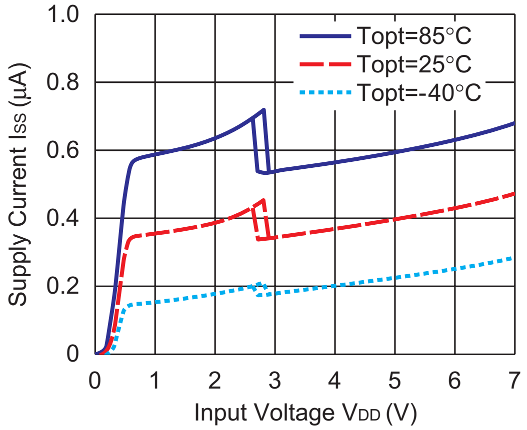
R3116x071A/C



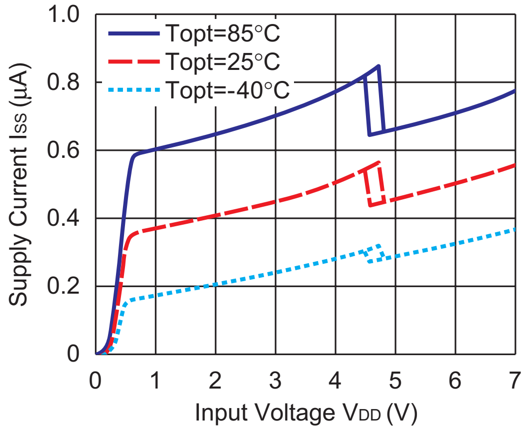
R3116x151A/C



R3116x271A/C

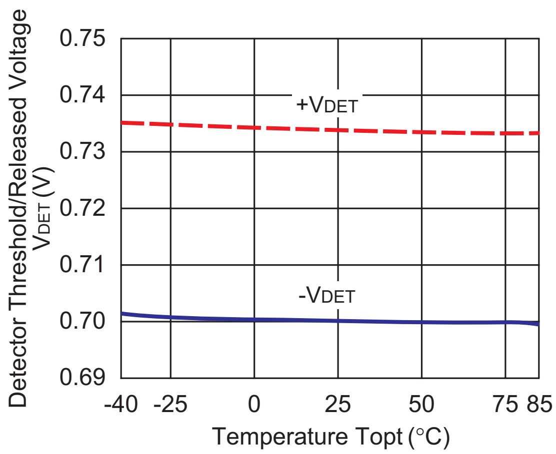


R3116x451A/C

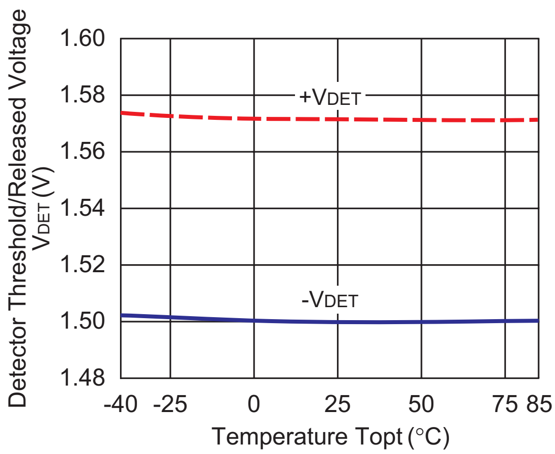


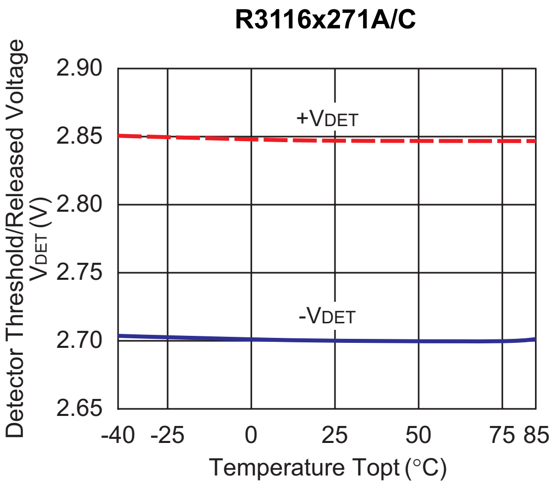
2) Detector Threshold vs. Temperature

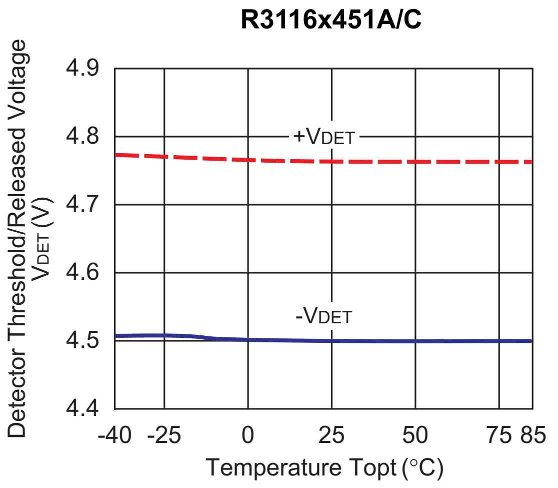
R3116x071A/C



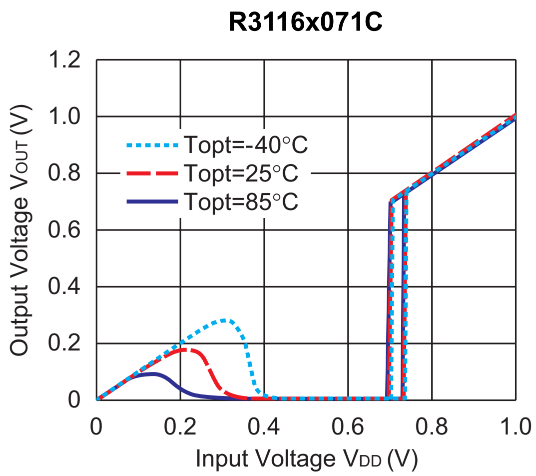
R3116x151A/C

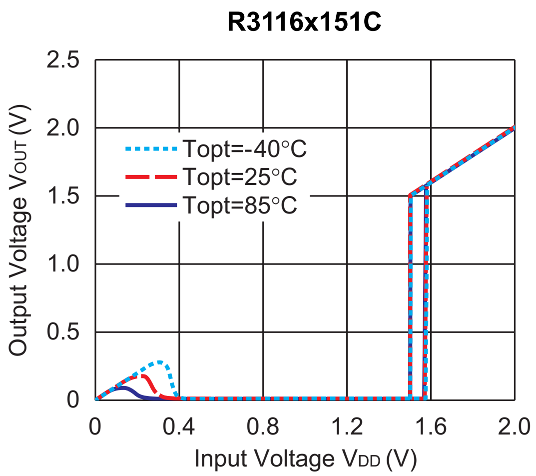


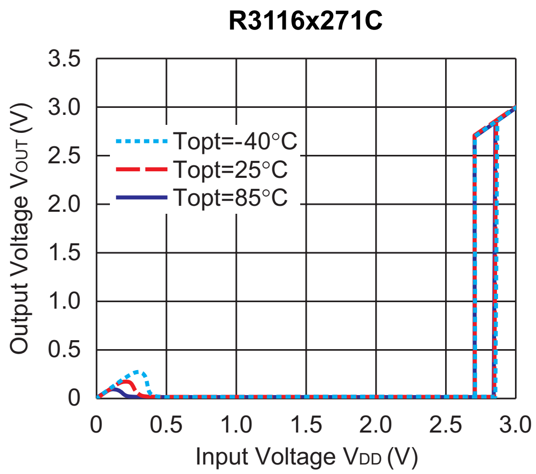


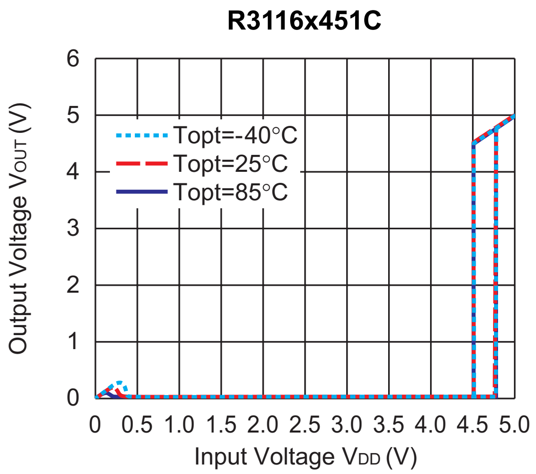


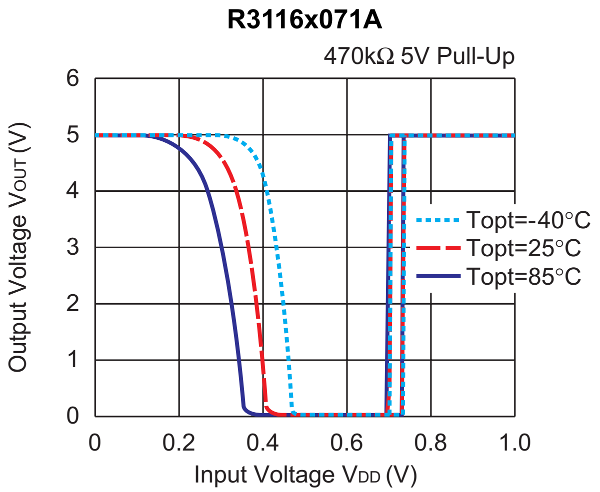
3) Output Voltage vs. Input Voltage

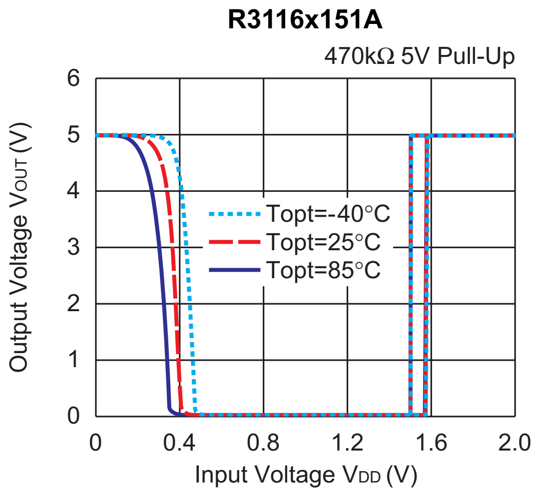


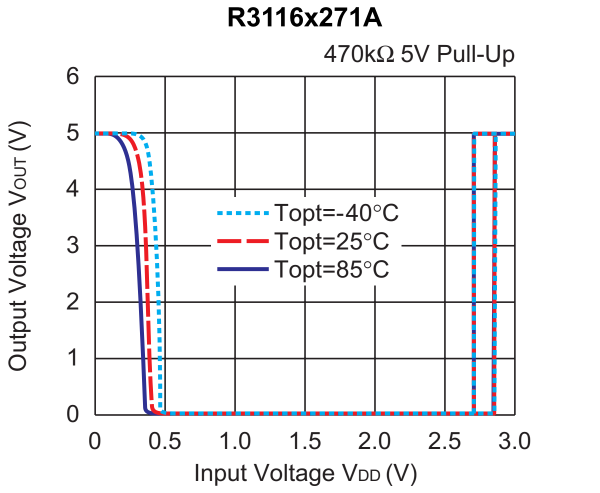


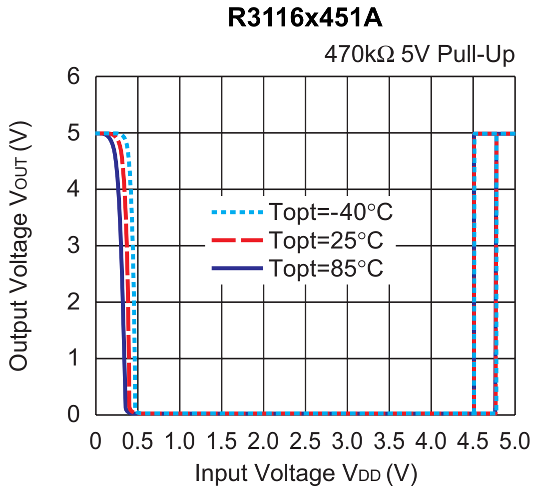




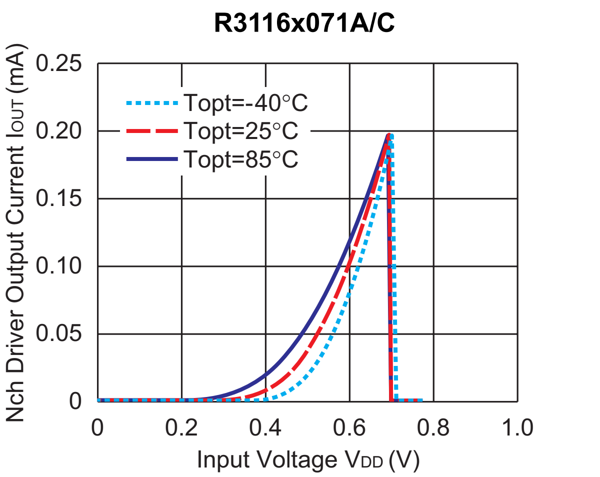


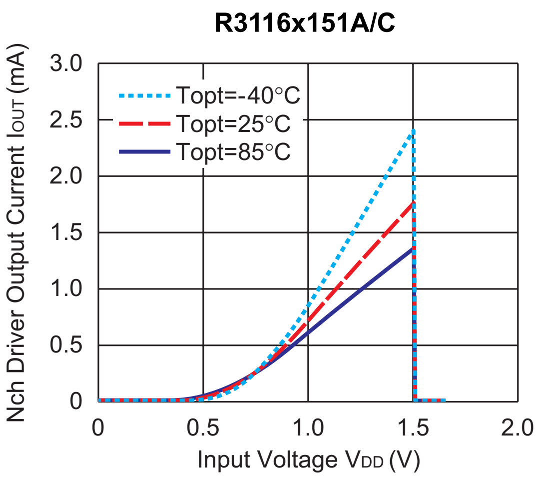




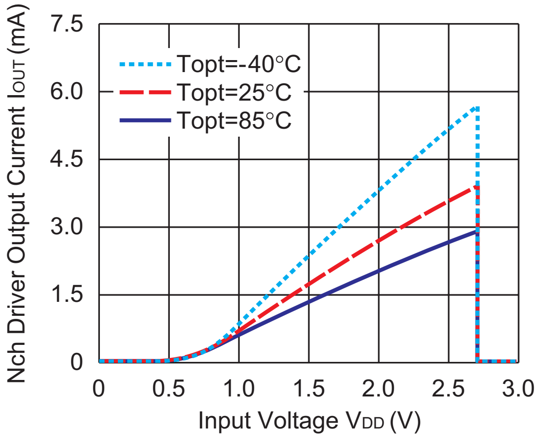


4) Nch Driver Output Current vs. Input Voltage (V_{DS}=0.5V)

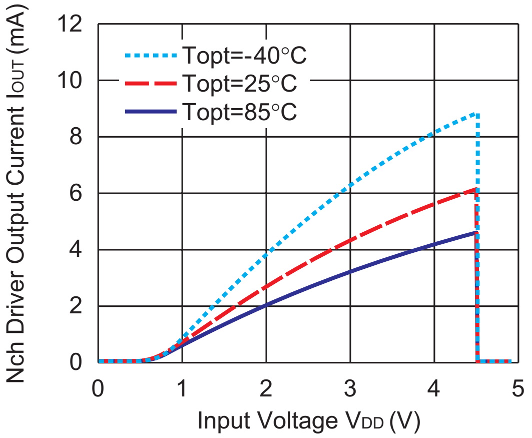




R3116x271A/C

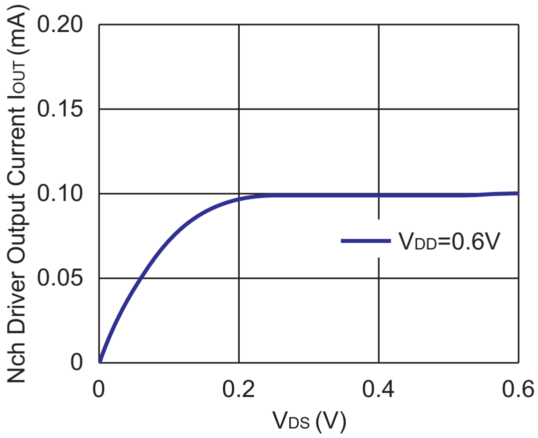


R3116x451A/C

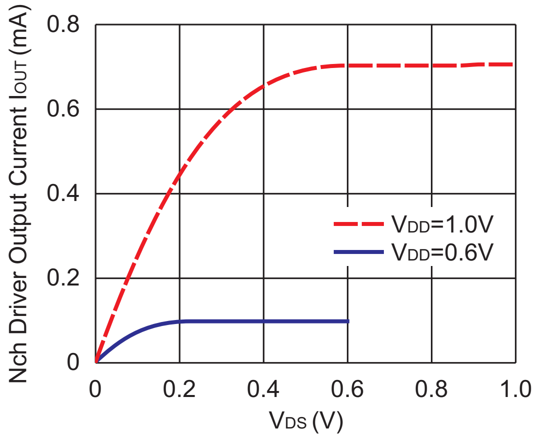


5) Nch Driver Output Current vs. VDS

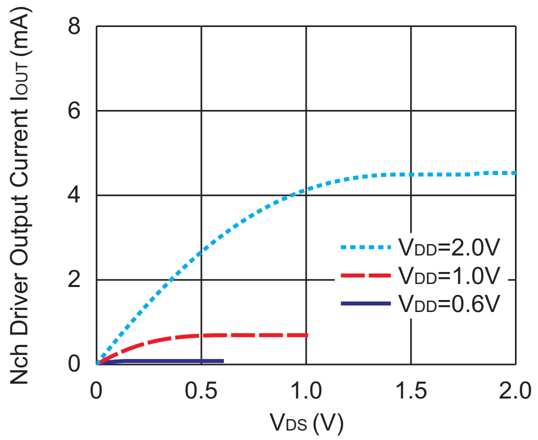
R3116x071A/C



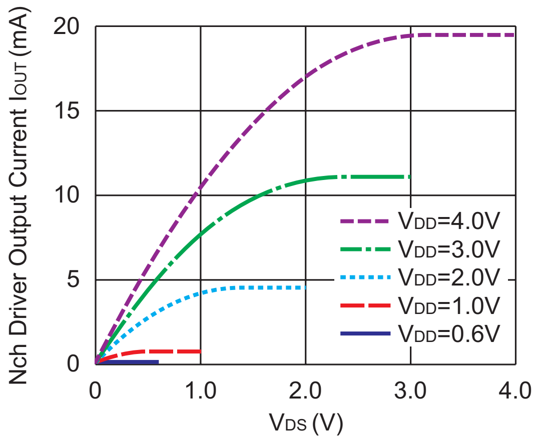
R3116x151A/C



R3116x271A/C

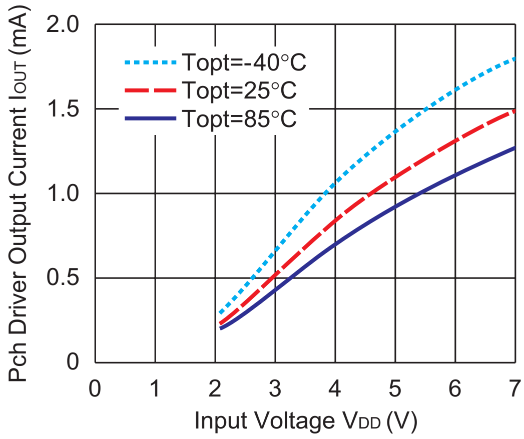


R3116x451A/C

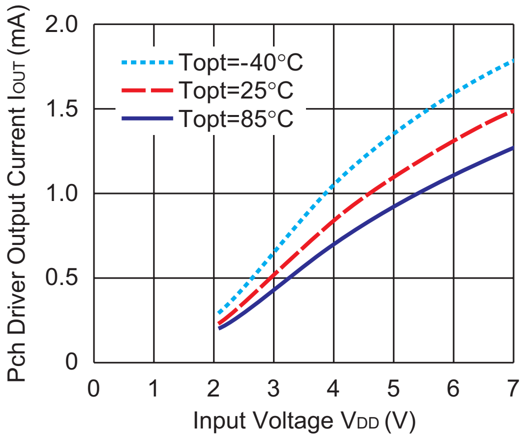


6) Pch Driver Output Current vs. Input Voltage (VDS=–2.1V)

R3116x071C



R3116x151C



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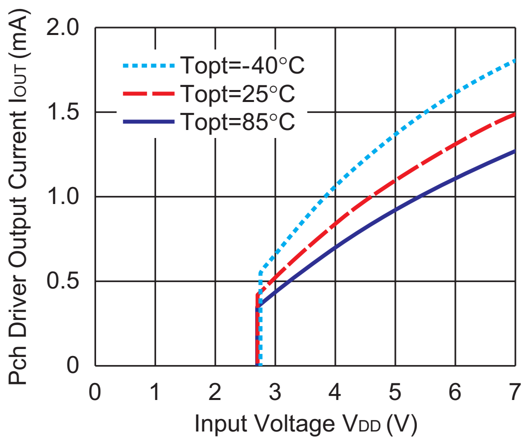
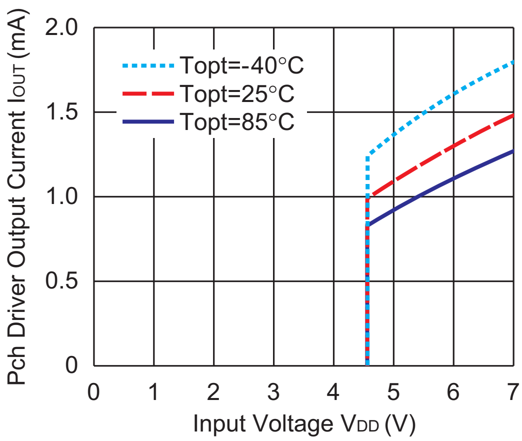
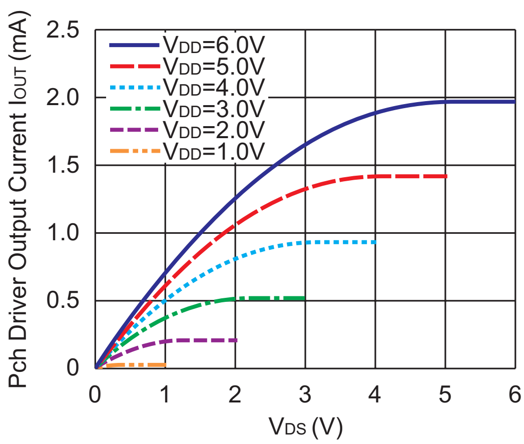


R3116x451C

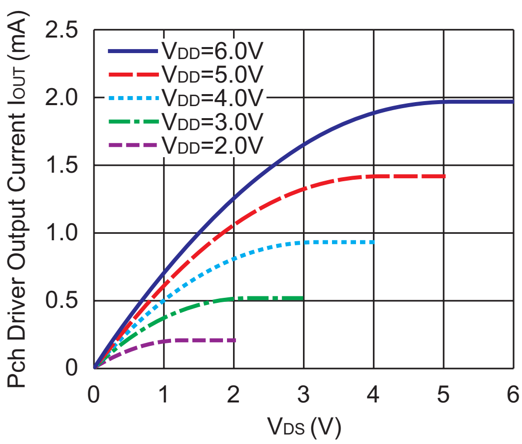


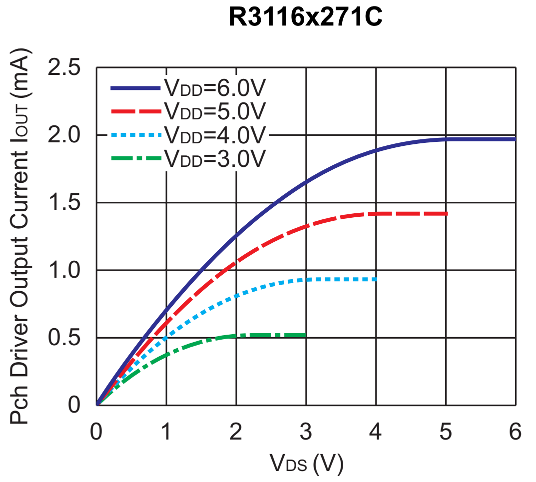
7) Pch Driver Output Current vs. VDS

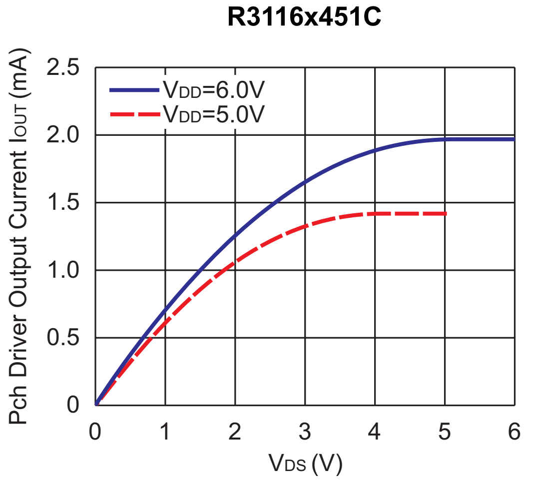
R3116x071C



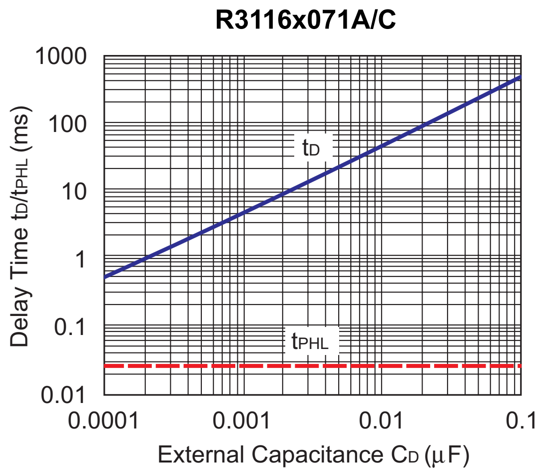
R3116x151C

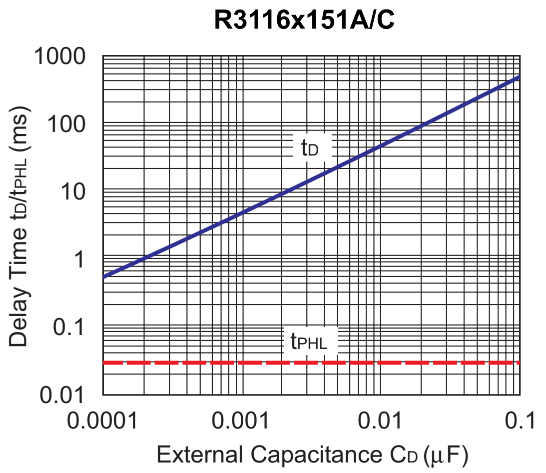


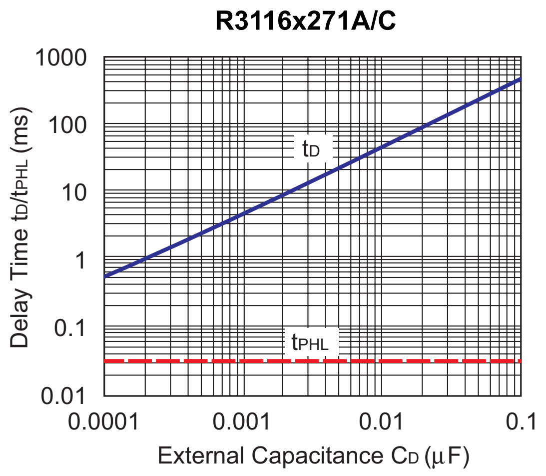


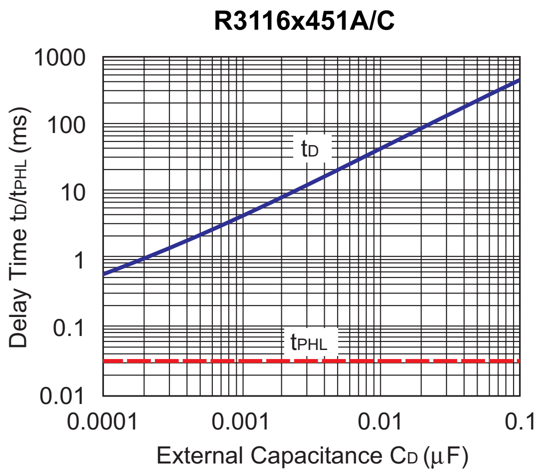


8) Output Delay Time vs. External Capacitance



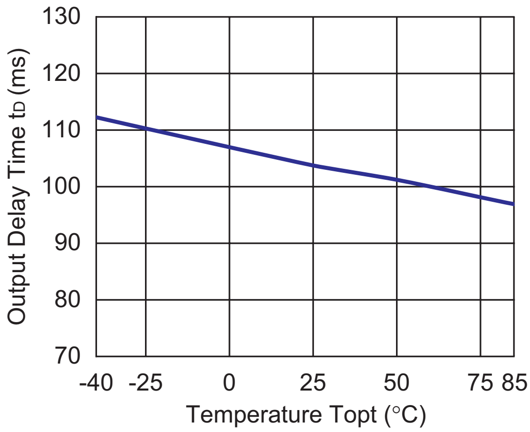




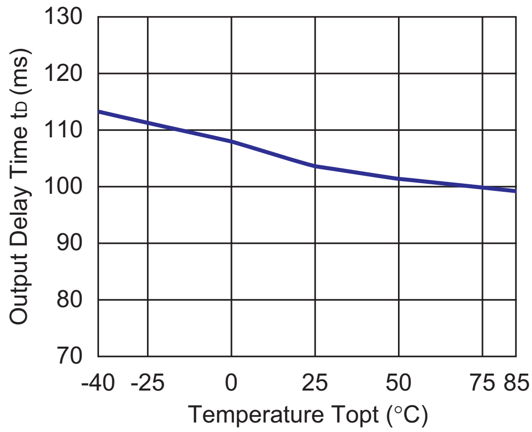


9) Output Delay Time vs. Temperature (C_D=22nF)

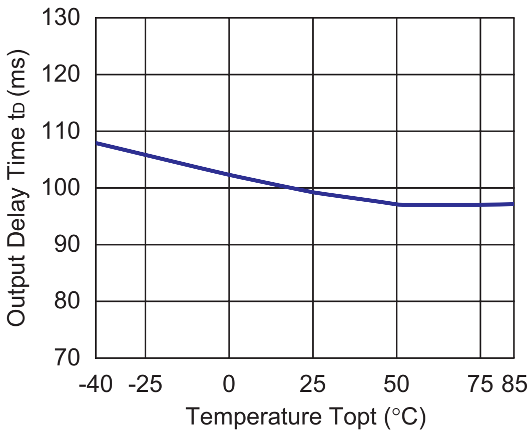
R3116x071A/C



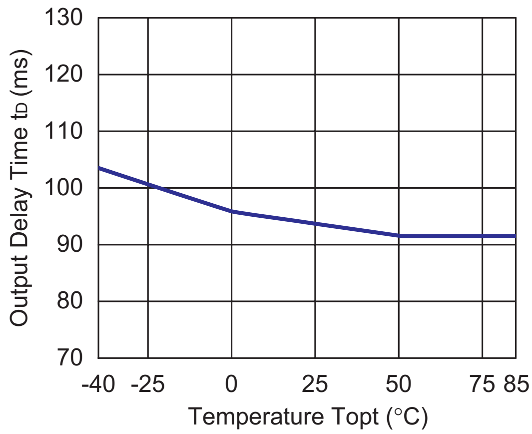
R3116x151A/C



R3116x271A/C



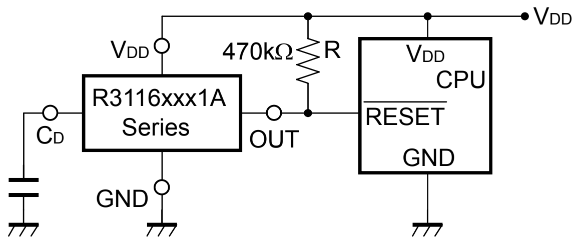
R3116x451A/C



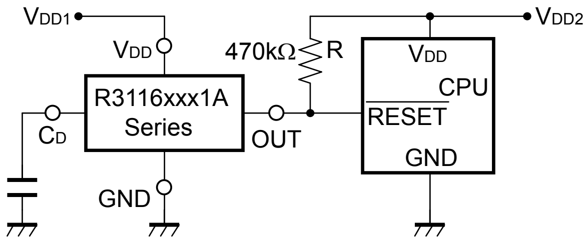
TYPICAL APPLICATION

- **R3116xxx1A CPU Reset Circuit 1 (Nch Open Drain Output)**

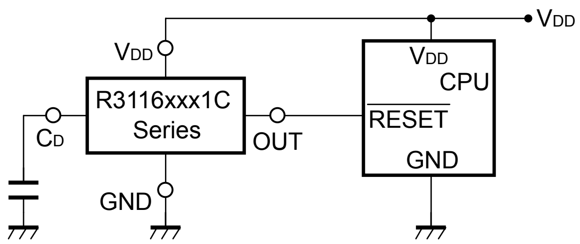
Case1. Input Voltage to R3116xxx1A is equal to Input Voltage to CPU



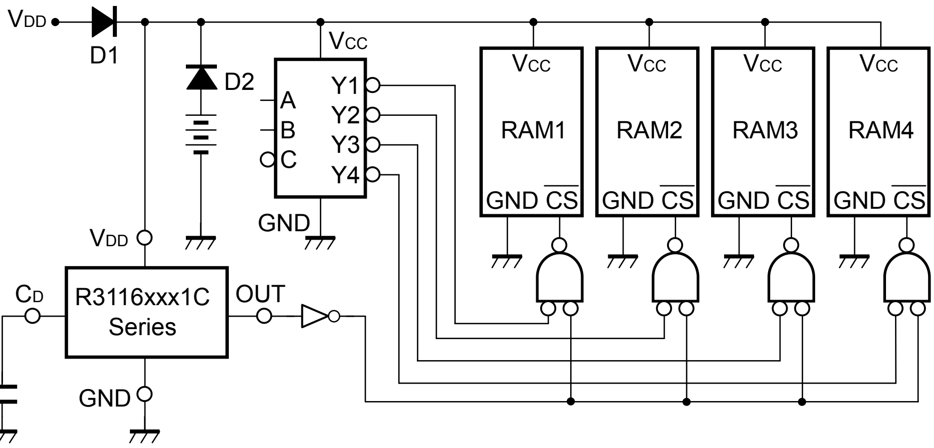
Case2. Input Voltage to R3116xxx1A is unequal to Input Voltage to CPU



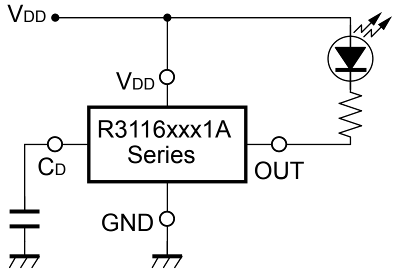
- **R3116xxx1C CPU Reset Circuit 2 (CMOS Output)**



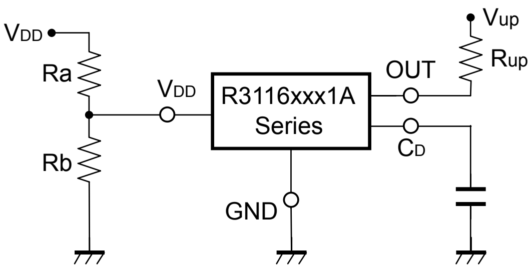
- **Memory Back-up Circuit**



- **Voltage level Indicator Circuit (lighted when the power runs out) (Nch Open Drain Output)**



- **Detector Threshold Adjustable Circuit 1 (Nch Open Drain Output)**

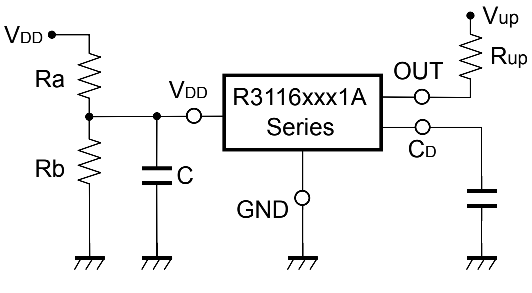


Adjustable Detector Threshold=(-V_{DET})×(Ra+Rb)/Rb

Hysteresis Voltage=(V_{HYS})×(Ra+Rb)/Rb

∗1) To prevent oscillation, set Ra ≦ 1kΩ, Rb ≦ 100Ω.
∗2) If the value of Ra is set excessively large, voltage drop may occur caused by the supply current of IC itself, and detector threshold and hysteresis voltage may vary.
∗3) If V_{up} and V_{DD} are connected, the voltage dropdown caused by R_{up}, may cause difference in the hysteresis voltage.

- **Detector Threshold Adjustable Circuit 2 (Nch Open Drain Output)**

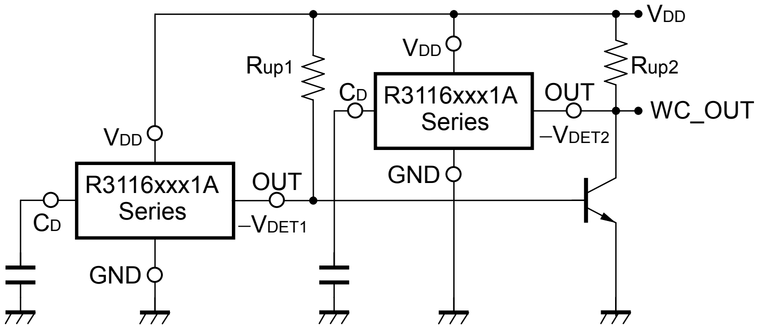


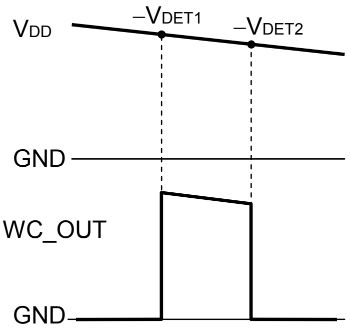
Adjustable Detector Threshold=(-V_{DET})×(Ra+Rb)/Rb

Hysteresis Voltage=(V_{HYS})×(Ra+Rb)/Rb

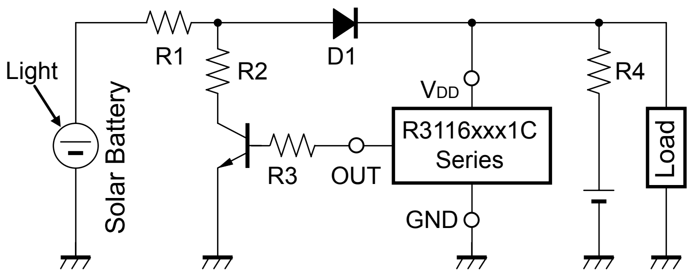
∗1) To prevent oscillation, set Ra ≦ 10kΩ, Rb ≦ 1kΩ, C ≧ 1μF.
∗2) If the value of Ra is set excessively large, voltage drop may occur caused by the supply current of IC itself, and detector threshold and hysteresis voltage may vary.
∗3) If V_{up} and V_{DD} are connected, the voltage dropdown caused by R_{up}, may cause difference in the hysteresis voltage.
∗4) If the value of Ra, Rb and C are set excessively large, the delay of the start-up may become too long.

- **Window Comparator Circuit (Nch Open Drain Output)**





- **Over-charge Preventing Circuit**



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TECHNICAL NOTES

When R3116xxx1A/C is used in Figure X, if the value of R1 is set excessively large, the dropdown voltage caused by the consumption current of IC itself, may vary the detector threshold and the release voltage. Also, if the value of R1 is set excessively large, there may be delay in start-up and may cause oscillation generated by cross conduction current.

When R3116xxx1A/C is used in Figure Y, if the value of R1 is set excessively large, the dropdown voltage caused by the consumption current of IC itself, may vary the detecor threshold and the released voltage. Also, if the value of R1 and R2 is set excessively large, there may be delay in start-up and may cause oscillation generated by cross conduction current.

When R3116xxx1A/C is used in Figure Z, if the value of R1 is set excessively large, the dropdown voltage caused by the consumption current of IC itself may vary the detector threshold and the release voltage. Also, if the value of R1 is set excessively large, there may be delay in start-up and may cause oscillation generated by cross conduction current. Furthermore, if the value of R1 is set large and the value of R2 is set small, released voltage level may shift and the minimum operating voltage may differ. If the value of R2 is set excessively small from R1, release may not occur and may cause oscillation.

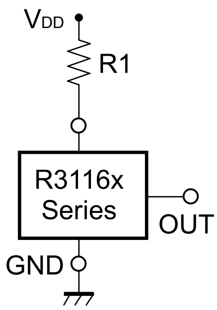

Figure X

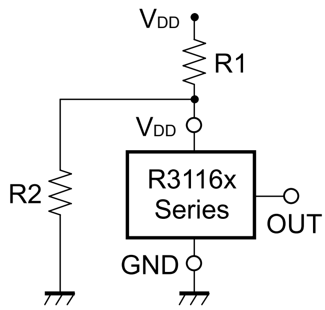

Figure Y

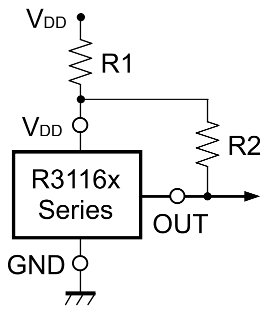

Figure Z

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