Version	Date/ Datum	Initiated by/ Veranlasser	Reason of modification / Grund der Änderung item, section / Position, Absatz
01	2006-10-13	Ghani Wee, Fakhariah (OPD - Oled FE Prod. Dev.)	New Specification

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Die Unterlage mit der Nr.:

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-

is no longer valid and must be sent to DocCenter.

Applicable Area - Scope / Gültigkeitsbereich	
Corporation:	OSRAM Opto Semiconductors
Location:	Penang
Cluster:	OLED
Unit:	OLED Module
SubUnit:	Full Moon
Process:	

Function / Funktion	Name & Dienststelle (in Druckschrift) Name & Department (printed letters)	Date / Datum	Signature / Unterschrift
Author/Change-Author	Ghani Wee, Fakhariah (OPD - Oled FE Prod. Dev.)	2006-10-13	sgd. per Livelink Workflow
Document Control	Lee, Lin-Yong (QAD - Quality Assurance Department); Bt Yusof, Noorrida (QAD - Quality Assurance Department)	2006-11-08; 2006-11-08	sgd. per Livelink Workflow
Head Of Org Unit	Lacey, David (OLM - OLED Mfg Support)	2006-11-07	sgd. per Livelink Workflow
Internal Customer	Chang, Chee Jia (OLM - OLED Mfg Support); Lui, MW (OLED Marketing)	2006-11-02; 2006-10-18	sgd. per Livelink Workflow
Order Fulfillment (OF)	Teo, Wei-Wei (OLM - OLED Mfg Support)	2006-10-16	sgd. per Livelink Workflow
Process Development	Lim, Kheng-Siang (OLN - OLED Engineering)	2006-10-13	sgd. per Livelink Workflow
Process Engineering	Sim, Lim-Thai (OLN - OLED Engineering)	2006-10-13	sgd. per Livelink Workflow
Product Development	Bin Abdul Manaf, Shahrol-Izzanni (OPD - Oled FE Prod. Dev.)	2006-10-16	sgd. per Livelink Workflow
Product Engineering	Ng, Chee-Pin (OLM - OLED Mfg Support)	2006-10-13	sgd. per Livelink Workflow
Production QM/QE	Lim, Lim-Ling (QED - Display QE)	2006-10-13	sgd. per Livelink Workflow

Revision Log

Rev	Description	Orig. By	ECN # / Date
A	New Spec	Fakhariah	

CONTENT Page

1. TITLE

1.1 Product Specification for HX2XX Full Moon OLED Module, 96X64, SSD0323, OS096064PK12MXXXXX

2. PURPOSE

2.1 This product specification is specifically for OLED Full Moon HX2XX.

3. SCOPE

3.1 This product specification is applicable to all HX2XX modules.

4. REFERENCE DOCUMENTS

4.1 C63062-H0200-A001-* Module Drawing (with bezel)
4.2 C63062-H0252-A001-* Module Drawing (without bezel)
4.3 SOLOMON SSD0323 128 x 80, 16 Gray scale Dot Matrix OLED/PLED Segment/Common Driver with Controller

5. OTHER REQUIREMENTS

5.1 FEATURES, FUNCTIONS, and REQUIREMENTS

5.1.1 Product Summary:

General OLED Module Description

Part Number	**OS096064PK12MXXXXX**
Display Format	96 columns x 64 rows
Pixel Pitch	0.265 (W) x 0.265 (H) mm
Pixel Size	0.235 (W) x 0.235 (H) mm
Display Diagonal	1.2“
Color	Monochrome – see table below for various colors
Grayscale	4 bits
Active Area	25.42 (W) X 16.94 (H) mm
Module size	Varies. See next section.
Glass size	33.85 (W) X 28.19 (H) X 3.49 (T) mm, including polarizer
Driver IC	SSD0323
Packaging/Interconnect	COF/ZIF

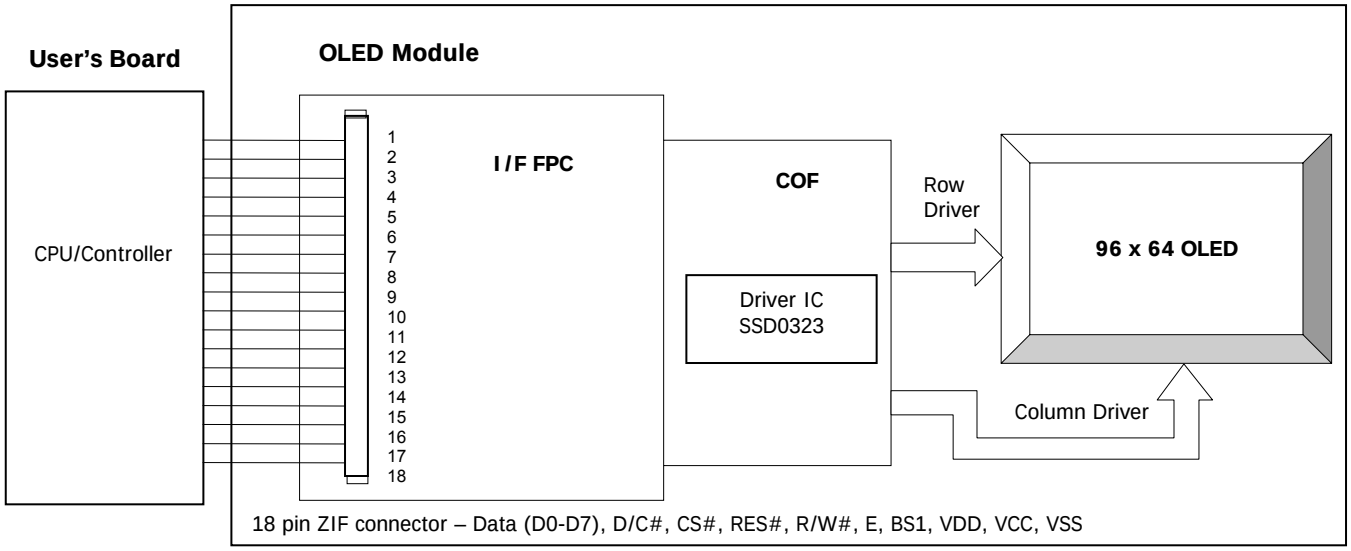
5.1.2 Part Number Options

Part Number Description

OS096064PK12Mxxxxx	Q Number	Color	Interface	Bezel	Module Size (excluding bezel tabs & flexes), mm	Factory Code
xxxxx = Y0A00	Q65110A1669	Elegance Yellow	Parallel	Metal	34.75 (W) X 29.89 (H) X 3.83 (T)	H0250
xxxxx = Y0Z00	Q65110A5715	Elegance Yellow	Parallel	Metal	34.75 (W) X 29.89 (H) X 3.83 (T)	HZ250
xxxxx = Y0A01	Q65110A1670	Elegance Yellow	Serial	Metal	34.75 (W) X 29.89 (H) X 3.83 (T)	H0251
xxxxx = Y0A10	Q65110A1712	Elegance Yellow	Parallel	None	33.85 (W) X 28.19 (H) X 3.59 (T)	H0252
xxxxx = Y0A11	Q65110A1710	Elegance Yellow	Serial	None	33.85 (W) X 28.19 (H) X 3.59 (T)	H0253
xxxxx = Y1A00	Q65110A3177	Light Green	Parallel	Metal	34.75 (W) X 29.89 (H) X 3.83 (T)	H0260
xxxxx = Y1A10	Q65110A3178	Light Green	Parallel	None	33.85 (W) X 28.19 (H) X 3.59 (T)	H0262
xxxxx = R1A00	Q65110A3430	Scarlet Red	Parallel	Metal	34.75 (W) X 29.89 (H) X 3.83 (T)	H1220
xxxxx = G1A00	Q65110A3431	Lime Green	Parallel	Metal	34.75 (W) X 29.89 (H) X 3.83 (T)	H1250
xxxxx = G2A00	Q65110A3432	Jungle Green	Parallel	Metal	34.75 (W) X 29.89 (H) X 3.83 (T)	H1260
xxxxx = O1A00	Q65110A3433	Tiger Orange	Parallel	Metal	34.75 (W) X 29.89 (H) X 3.83 (T)	H1270

5.1.3 Electrical Characteristics

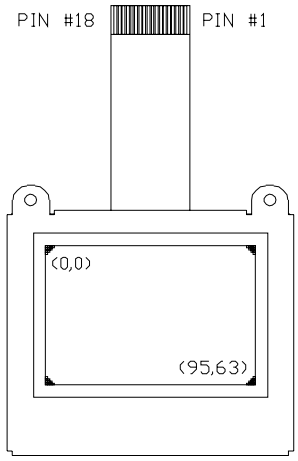
Functional Block Diagram



Overall block diagram of display module assembly and interface

5.1.4 Graphic Area Pixel Mapping

Rows are designed in the interleave configuration. The COM re-map command allows for proper orientation of the image displayed.



Pixel mapping and glass design layout (top plated contacts)

5.1.5 Duty Cycle

The rows are multiplexed and will operate at a nominal duty cycle of 1/64.The default duty cycle is 1/80. A software command must be used to adjust during initialization.

5.1.6 Interface Pin Out

There are two interface pin out options corresponding to the parallel and serial interface requirements. The interface is factory-set by jumper JP1 on the FPC; JP1 = 1 for parallel I/F, JP1 = 0 for serial I/F. For the parallel I/F version only, the user can select the interface protocol using pin #3 BS1 (for Motorola 68 series or Intel 80 series).

5.1.6.1 ZIF Connection Pin Out

	Parallel I/F		*Serial I/F*	
Pin No.	**Name**	**Description**	**Name**	**Description**
1	CS#	Chip Select	CS#	Chip Select
2	RES#	Reset	RES#	Reset
3	BS1	Parallel I/F protocol Low: 68 series; High: 80 series	BS1	Set to Low or connect to VSS
4	D/C#	High: Data in GDDRAM Low: Command	D/C#	High: Data in GDDRAM Low: Command
5	R/W# (WR#)	Read/Write selector for 68 series; Write strobe for 80 series	NC	No connect
6	E (RD#)	E clock for 68 series; RD strobe for 80 series	NC	No connect
7	D0	Parallel Data 0	SCLK	Serial Clock Input
8	D1	Parallel Data 1	SDIN	Serial Data Input
9	D2	Parallel Data 2	NC	No connect
10	D3	Parallel Data 3	NC	No connect
11	D4	Parallel Data 4	NC	No connect
12	D5	Parallel Data 5	NC	No connect
13	D6	Parallel Data 6	NC	No connect
14	D7	Parallel Data 7	NC	No connect
15	NC	No connect	NC	No connect
16	VDD	Logic Power	VDD	Logic Power
17	VCC	OLED Power Supply	VCC	OLED Power Supply
18	VSS	Ground	VSS	Ground

5.1.7 Absolute Maximum Ratings

Absolute Maximum Ratings

Symbol	Description	Range	Unit
VDD	Supply Voltage for logic	-0.3 to +4.0	V
VCC/ VLL	Supply Voltage for driver	0.0 to +16.0	V
Vin	Input Voltage	VSS-0.3 to VDD+0.4	V
Ta	Operating Temperature	-30 to +70	ºC
Tstg	Storage Temperature Range	-40 to +70	ºC

5.1.8 DC Characteristics of Complete Module

(-30ºC to +70ºC Temperature Range, except as noted)

Recommended DC Operating Conditions

Description		Symbol	MIN	TYP	MAX	Units
Operating voltage for logic		VDD	2.4	3.0	3.5	V
OLED driver input voltage		VCC	12.0	12.5	13.0	V
Operating Current (logic)		IDD	-	-	650.0	µA
Operating Current (OLED), All pixels ON, Luminance at typical value (100nits)		ICC(1)	17.0	18.0	20.0	mA
		ICC(2)	-	18.0	20.0	mA
		ICC(3)	25.0	27.0	28.0	mA
Driver Sleep Mode Current (+25C)		ISL	-	-	5.0	µA
DC-DC Voltage converter input voltage (Optional, not available in all p/n)		VDD	-	-	-	V
Logic Input voltage	High	VIH	.8 *VDD	-	VDD	V
	Low	VIL	0	-	.2*VDD	V
Logic output voltage	High (IOH=0.5mA)	VOH	.9 *VDD	-	VDD	V
	Low (IOL=0.5mA)	VOL	0	-	.1*VDD	V

Note :

ICC(1): operating current for :
H025X-OS096064PK12MY0AXX and HZ250-OS096064PK12MY1Z00

ICC(2): operating current for :
H026X-OS096064PK12MY1AXX

ICC(3): operating current for :
H12X0-OS096064PK12MXXA00

5.1.9 Power Consumption

(VDD= 3.0V, VCC = 12.5V, Frame Frequency = 75 Hz, unless otherwise stated)

Power Consumption

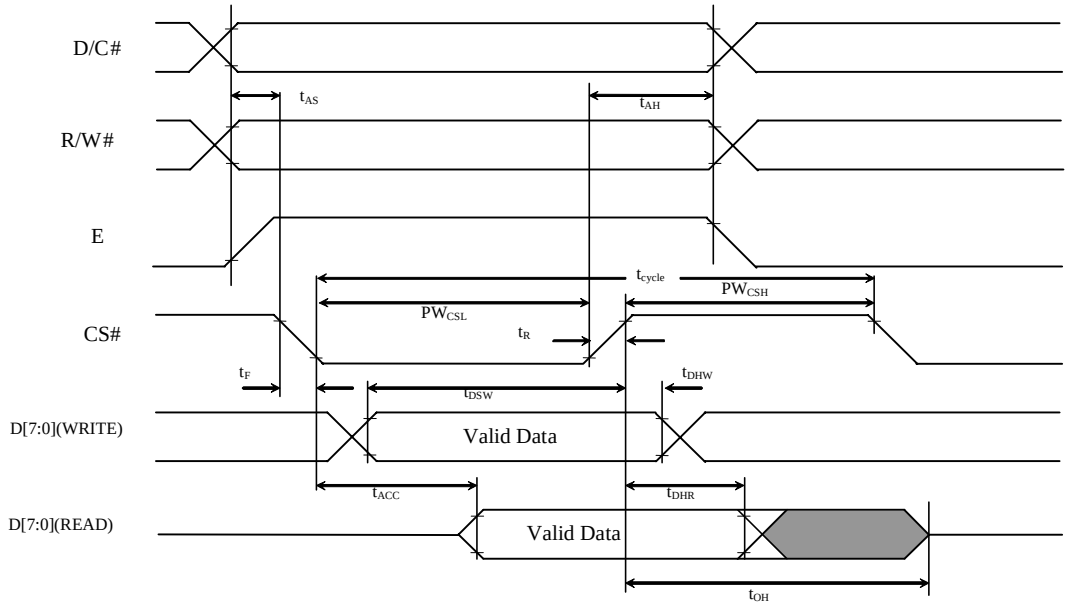
		Typical Power Consuption* (mW), Dual supply (VDD, VCC) ±10%				
Model	**Typical Luminace** Cd/m²	**Power Save mode (Sleep mode)**	**All pixels ON @ typical brightness**	**10% ON @ typical brightness**	**10% ON @ 15% of typ. brightness**	**2% ON @ 15% of typ. brightness**
Elegance Yellow	100	0.015	211	26	8	4
Light Green	125	0.013	240	30	8	4
Lime Green	145	0.013	340	40	9	4
Jungle Green	40	0.013	340	40	9	4
Tiger Orange	50	0.013	340	40	9	4
Scarlet Red	18	0.013	340	40	9	4

5.1.10 AC Timing Characteristics

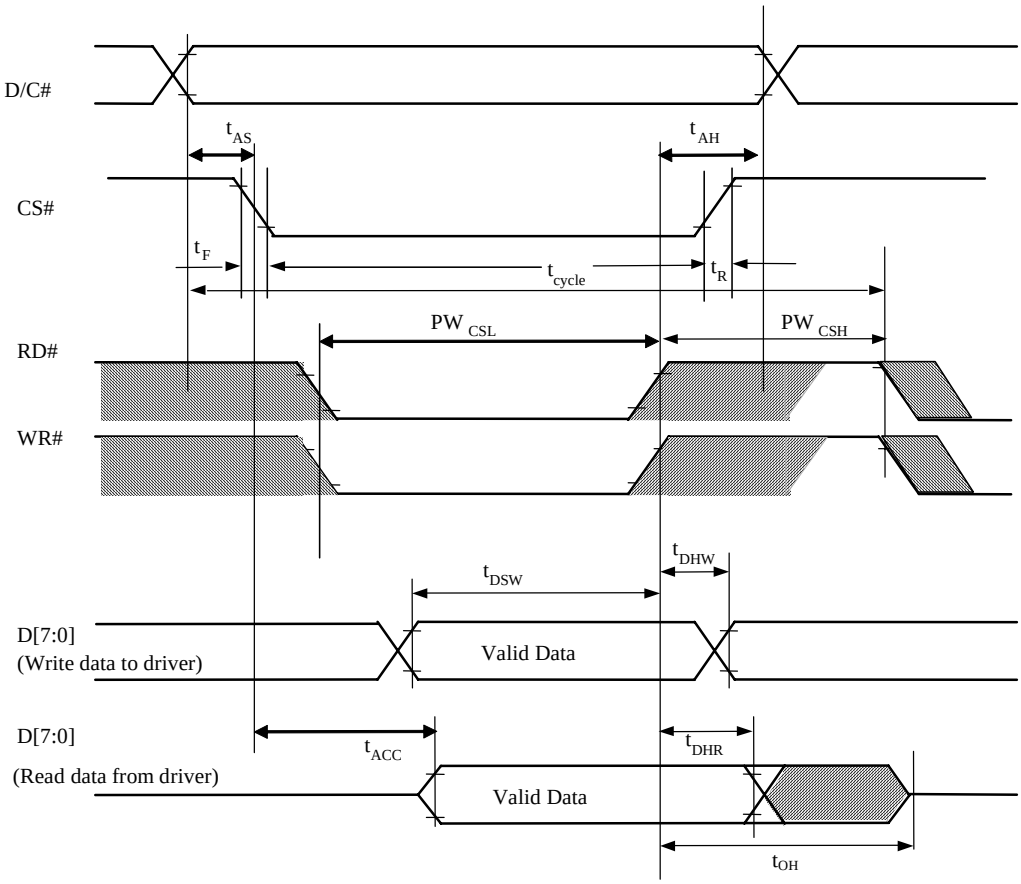
5.1.10.1 Parallel Interface Timing Characteristic

Parallel Interface Timing Characteristics

Description	Symbol	Min.	Typ.	Max.	Unit
Clock Cycle Time	tcycle	300	-	-	ns
Address Setup Time	tAS	0	-	-	ns
Address Hold Time	tAH	0	-	-	ns
Write Data Setup Time	tDSW	40	-	-	ns
Write Data Hold Time	tDHW	15	-		ns
Read Data Hold Time	tDHR	20	-		ns
Output Disable Time	tOH	-	-	70	ns
Access Time	tACC	-	-	140	ns
Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	PW CSL	120 60	-		ns
Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	PWCSH	60 60	-		ns
Rise Time	tR	-	-	15	ns
Fall Time	tF	-	-	15	ns
Frame Frequency	tFRM	70	75	85	Hz



Parallel Interface Timing Diagram for 68 Series MPU

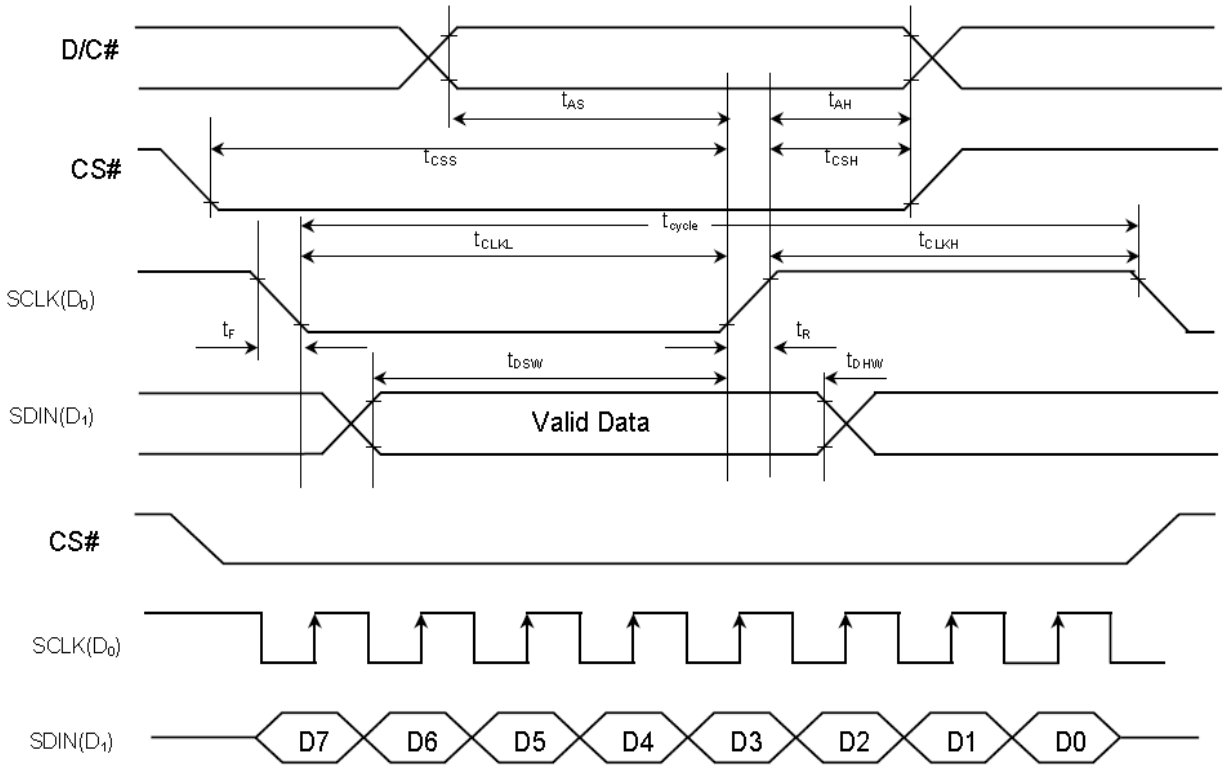


Parallel Interface Timing Diagram for 80 Series MPU

5.1.10.2 Serial Interface Timing Characteristic

Serial Interface Timing Characteristics

Description	Symbol	Min.	Typ.	Max.	Unit
Clock Cycle Time	tcycle	250	-	-	ns
Address Setup Time	tAS	150	-	-	ns
Address Hold Time	tAH	150	-	-	ns
Chip Select Setup Time	tCSS	120	-	-	ns
Chip Select Hold Time	tCSH	60	-	-	ns
Write Data Setup Time	tDSW	100	-	-	ns
Write Data Hold Time	tDHW	100	-	-	ns
Clock Low Time	tCLKL	100	-	-	ns
Clock High Time	tCLKH	100	-	-	ns
Rise Time	tR	-	-	15	ns
Fall Time	tF	-	-	15	ns
Frame Frequency	tFRM	70	75	85	Hz



Serial Interface Timing Diagram

5.2 Display Programming

5.2.1 Programming

Refer to specification: Solomon SSD0323 OLED/PLED Segment/Common Driver with Controller CMOS

5.2.2 Initialization

After power up, the commands specified in the Initialization Table below must be executed during initialization

Initialization Sequence

Command	Code	Default on POR	Initialization For module (A)	Initialization For module (B)	Initialization For Module (C)
Set Column Address	15	00	default	default	default
		3F	2F	2F	2F
Set Row Address	75	00	default	default	default
		4F	3F	3F	3F
Set Contrast Control	81	40	33*	40*	60*
Set Current Range	84~86	84 (Quarter)	86 (Full)	86 (Full)	86 (Full)
Set Re-map	A0	00	52	52	52
Set Display Start Line	A1	00	00	00	00
Set Display Offset	A2	00	40	40	40
Set Multiplex Ratio	A8	4F	3F	3F	3F
Set Display ON or OFF		AE	AF	AF	AF
Set Row Period	B2	25	46	46	46
Set Master Configuration, DC-DC	AD	03	02	02	02
Set Bias Current Setting for DC-DC	CF	F0	default	default	default
Set Pre-charge Compensation Enable	B0	08	default	default	default
Set Pre-charge Compensation Level	B4	00	default	default	default
Set Clock Divide	B3	02	41	41	41
Set Phase Length	B1	P1 = 3, P2 = 5	P1 = 2, P2 = 2	P1 = 2, P2 = 2	P1 = 2, P2 = 2
Set VSL	BF	0E	0D	0D	0D
Set VcomH	BE	11	00	03	08
Set Vprecharge	BC	18	0B	11	14
Set Gray Scale Table			See Sample Gray Scale Settings	See Sample Gray Scale Settings	See Sample Gray Scale Settings

Note: * All in Hex

Note: * This setting represents maximum luminance for proper operation of the display. Lower setting can be used for dimming. Higher setting will adversely affect the operating lifetime as defined in this specification.

Module (A) : H025X-OS096064PK12MY1AXX and HZ250-OS096064PK12MY1Z00
Module (B) : H026X-OS096064PK12MY1AXX
Module (C) : H12X0-OS096064PK12MXXA00

Sample Gray Scale Settings (Decimal)

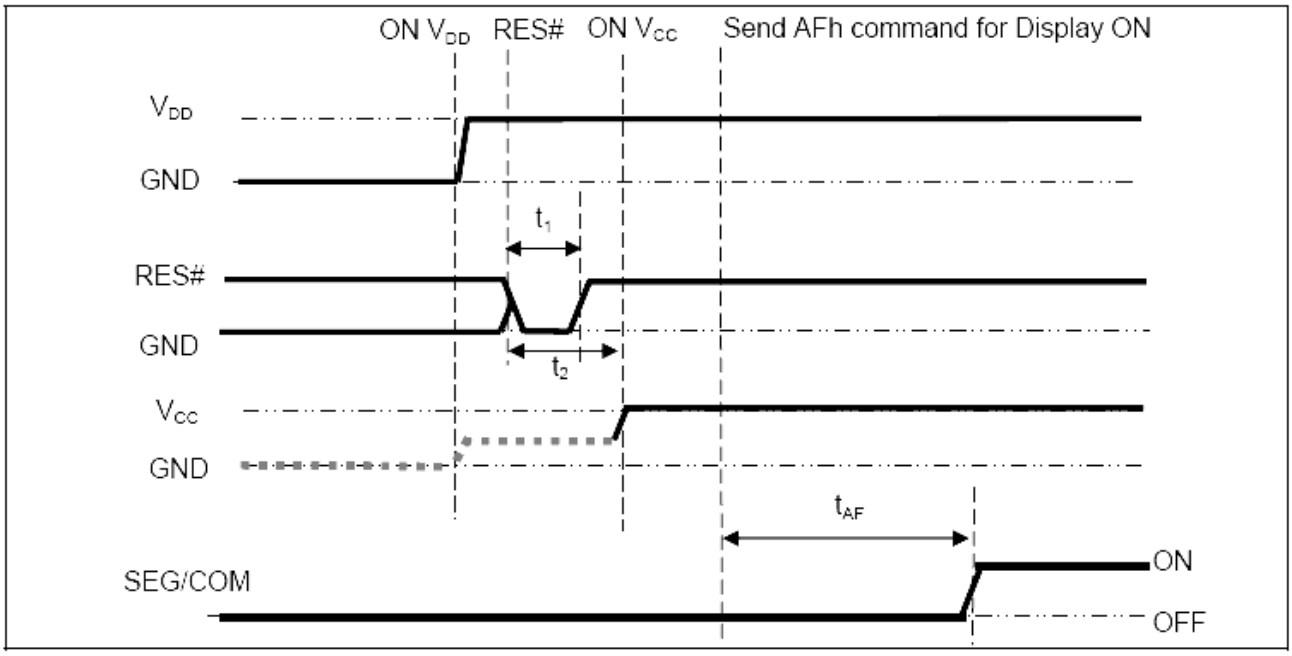
GS level	Phase 1	Phase 2	S/W Set	GS Pulse	Total DCLK
L0	2	2	0	0	4
L1	2	2	1	1	5
L2	2	2	1	3	7
L3	2	2	1	5	9
L4	2	2	2	8	12
L5	2	2	2	11	15
L6	2	2	2	14	18
L7	2	2	3	18	22
L8	2	2	3	22	26
L9	2	2	4	27	31
L10	2	2	4	32	36
L11	2	2	5	38	42
L12	2	2	5	44	48
L13	2	2	6	51	55
L14	2	2	6	58	62
L15	2	2	7	66	70

5.3 Power Up and Power Down Sequence:

To protect the OLED panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources turn on/off.

5.3.1 Power-Up Sequence:

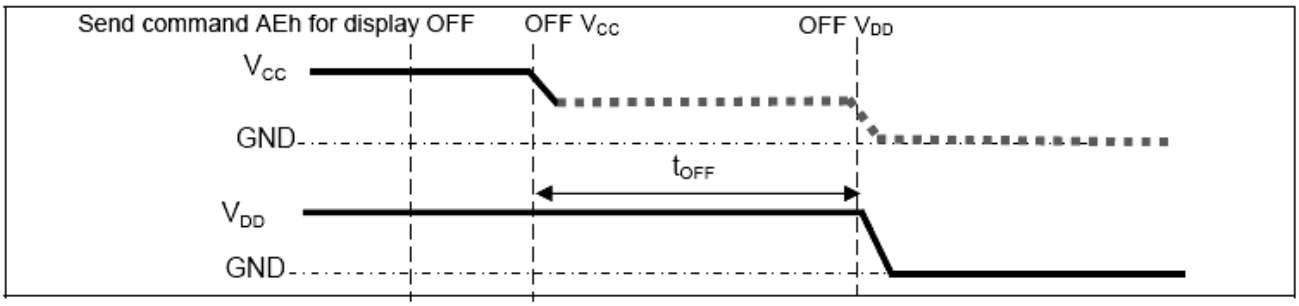
I. Power-Up Vdd
II. After V_{DD} become stable, set RES# pin LOW (logic LOW) for at least 3us (t_1) and then HIGH (logic HIGH)
III. After set RES# pin LOW (logic LOW), wait for at least 3us (t_2). Then Power ON V_{CC}
IV. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 30ms (t_{AF}).



Power-Up Diagram

5.3.2 Power-Down Sequence:

I. Send command AEh for Display off
II. Wait until panel discharges completely
III. Power down Vcc
IV. Wait for t_{OFF}. Power OFF V_{DD}. (where Minimum t_{OFF}=0ms, Typical t_{OFF}=30ms)



Power-Down Diagram

5.4 OPTICAL CHARACTERISTICS (Ta = 25°C, VCC = 12.5V, VDD = 3.0V, unless otherwise stated)

Optical & Operating Lifetime Characteristics

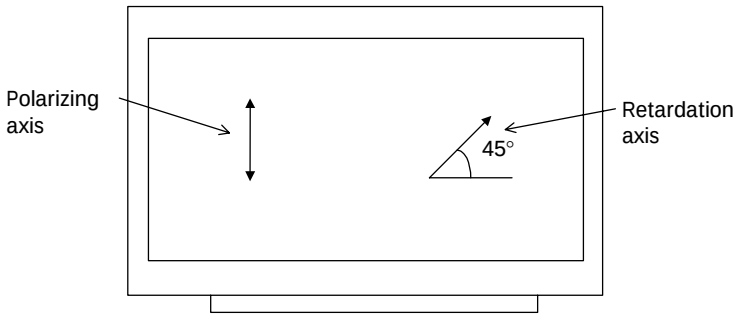
	Condition	Min.	Typ.	Max	Unit
Contrast ratio	$\upsilon = \phi = 0°$	-	2000	-	-
	In Direct Sun light	1.05	-	-	
Brightness Uniformity	$\upsilon = \phi = 0°$	-	-	+20	%
Visible Flickers	$\upsilon = \phi = 0°$	-	None	-	-
Cross Talk (Brightness variation of OFF pixels)	$\upsilon = \phi = 0°$	-	-	10	%

Color Coordinates and Initial Luminance

Product	Color	X color coordinate 1931 CIE, ±0.02	X color coordinate 1931 CIE, ±0.02	Typical Initial Luminance, cd/m²			Operating Lifetime * Hours, @25°C
				Min.	Typ.	Max	
H025X-OS096064PK12MY0AXX	Elegance Yellow	0.455	0.540	90	100	140	40K
HZ250-OS096064PK12MY0A00	Elegance Yellow	0.455	0.540	90	100	140	40K
H026X-OS096064PK12MY1AXX	Light Green	0.440	0.560	120	125	135	40K
H1250-OS096064PK12MG1A00	Lime Green	0.370	0.620	140	145	150	10K
H1260-OS096064PK12MG2A00	Jungle Green	0.250	0.730	35	40	45	10K
H1270-OS096064PK12MO1A00	Tiger Orange	0.630	0.370	45	50	55	10K
H1220-OS096064PK12MR1A00	Scarlet Red	0.690	0.310	15	18	20	10K

*Operating Lifetime is Time to Half Luminance; based on the display operated at 25°C at typical brightness level with specified software settings, until reaching 50% of initial luminance.

5.4.1 Polarizing angle



Orientation of OLED polarizer angle

5.4.2 Mechanical Characteristics

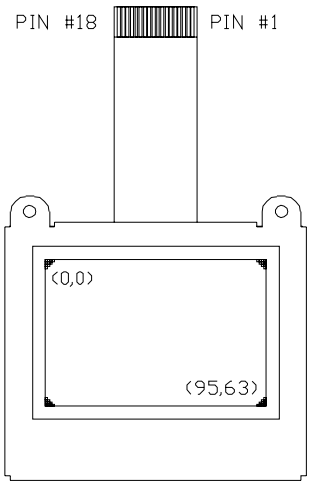
5.4.2.1 Interconnections

The display module should be electrically connected to a controller on the user's board through the 18-contact pad ZIF tail.

5.4.2.2 Recommended Mating Connectors

5.4.2.2.1 Top Contact: HIROSE: FH12A-18S-0.5SH, or equilvalent

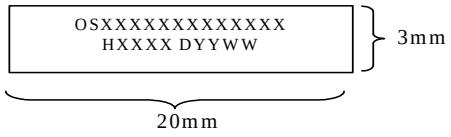
5.4.2.2.2 Bottom Contact: Molex: 52893-1890, HIROSE: FH12-18S-0.5SH, or equilvalent



Orientation of ZIF connector tail pin out

5.4.2.3 Product Marking

Parts are marked as shown below in figure



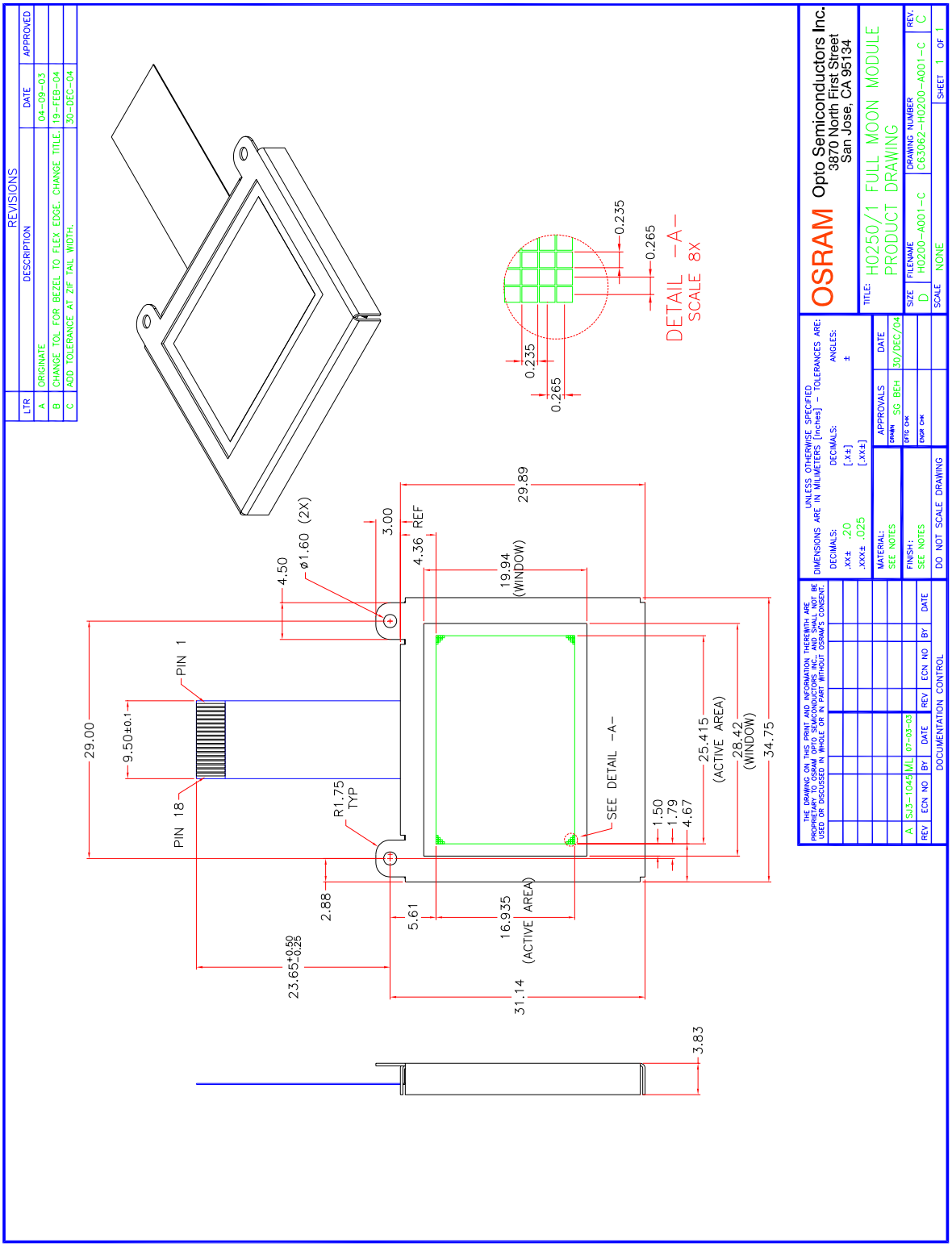
Legend
OSRAM P/N & Code
Date Code
D: Day; YY: Year
WW: PC Week

Description of part label marking requirements

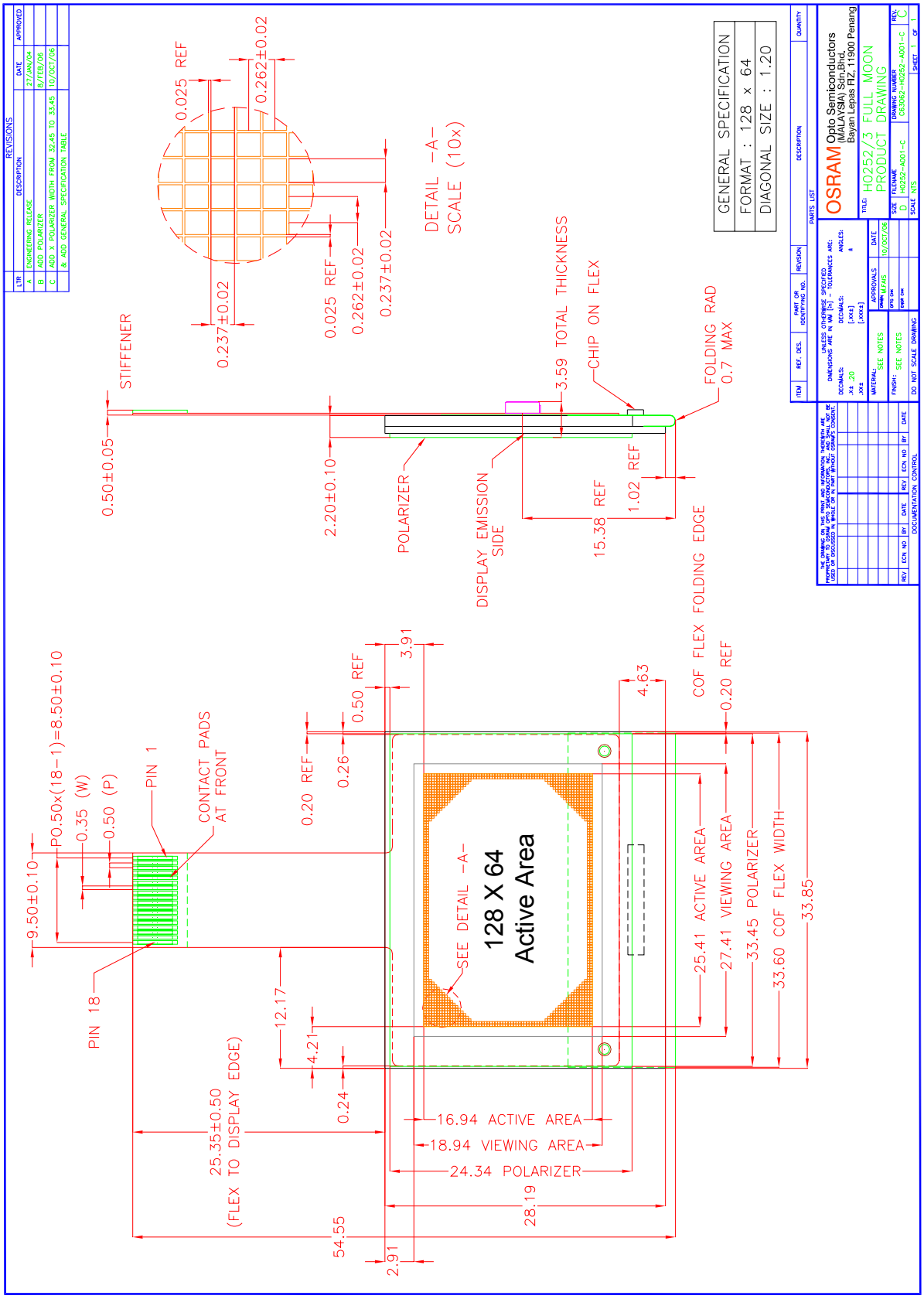
5.5 Module Mechanical Drawing

The mechanical drawings shown in below figures are provided for reference

Module drawing for parts with bezel



Module drawing for parts without bezel



6. QUALIFICATION TESTING

For reference, the main qualification tests and test criteria done on the OLED module are indicated below in Tables, respectively

OLED Module Internal Qualification Tests

Test	Condition	Duration
High Temperature and Humidity Bias (THB)*	60°C / 90% RH	250 hrs
High Temperature Operating (ELT)*	70°C	336 hrs
Powered Temperature Cycle (PTC)*	-30°C / 70°C; 30 min. dwell time; 15 min. transition time	60 cycles
Thermal Shock (TSK)	-40°C / 85°C; 45 min. dwell time; 15 sec. Transition time	100 cycles
Low Temperature Storage (LTS)	-40°C	336 hrs
High Temperature Storage (HTS)	70°C	336 hrs
Low Air PressureLAT **	15kPa 25°C (0.15bar)	16hrs
Mechanical Vibration**	10-58hz 0.75mm 58-150Hz 10g 1oct/min	10 sweeps per X, Y, Z direction
Mechanical Shock**	11ms half sine 100g peak	6 shocks per X, Y, Z direction
Mechanical Bump**	6ms half sine 40g Peak	1000 bumps per X, Y, Z direction

Note 1: The modules are powered for these tests, with a standard OSRAM pattern (50% emission ratio)

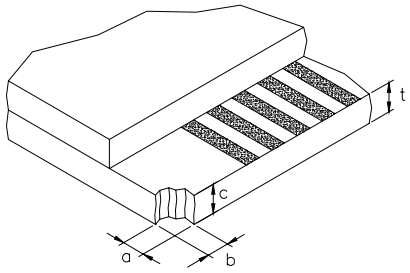
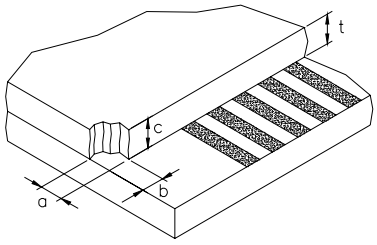
** ***Note 2***: These mechanical tests are performed on a representative part of the same product family.

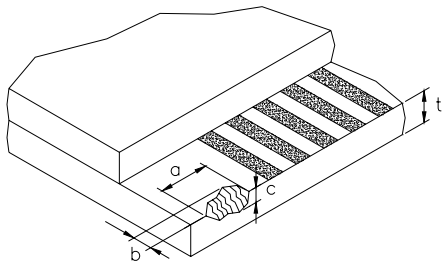
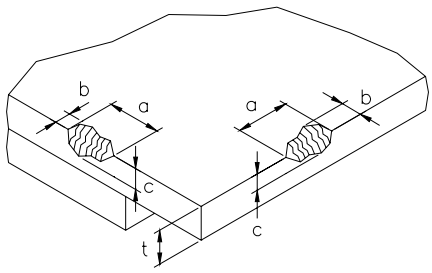
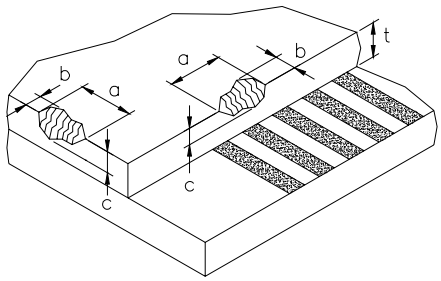
OLED Module Qualification Test Criteria

Acceptance Criteria (without polarizer):	Test Patterns for Powered Tests:
< 50% luminance loss after test	Checkerboard pattern
5 point luminance uniformity <20%	Inverse Checkerboard pattern
No mechanical failure	All pixels On
No electrical failure	All pixels Off
Pixel gap (initial + growth) $\leq$ 30% of pitch	

7. COSMETIC CRITERIA

<table>
<tr><th>Items</th><th>Criterion for Defects</th><th>Defect Type</th></tr>
<tr><td>Black / bright spot, particle, pin-hole (on the glass / polarizer), dent on polarizer</td><td>Within Viewing Area
<table><tr><th>Size Φ (mm)</th><th>Acceptable number</th></tr><tr><td>Φ ≤ 0.1</td><td>Not counted</td></tr><tr><td>0.1 ≤ Φ ≤ 0.2</td><td>3</td></tr><tr><td>Φ > 0.2</td><td>0</td></tr></table>* Φ = (Long diameter + Short diameter)/2</td><td>Minor</td></tr>
<tr><td>Scratches / lines on the polarizer</td><td>Within Viewing Area
<table><tr><th>Size Φ (mm)</th><th>Acceptable number</th></tr><tr><td>W≤ 0.1</td><td>Not counted</td></tr><tr><td>L ≤ 2, 0.1 < W ≤ 0.2</td><td>3</td></tr><tr><td>W > 0.2</td><td>0</td></tr></table></td><td>Minor</td></tr>
<tr><td>Polarizer Bubble</td><td>Reject if bubble is observed with naked eyes at 30cm distance. with the following criteria

Within Viewing Area
<table><tr><th>Size Φ (mm)</th><th>Acceptable number</th></tr><tr><td>Φ ≤ 0.2</td><td>Not counted</td></tr><tr><td>0.2≤Φ ≤ 0.3</td><td>3</td></tr><tr><td>0.3 < Φ</td><td>0</td></tr></table>Outside Viewing Area – IGNORE</td><td>Minor</td></tr>
<tr><td>Polarizer coverage</td><td>Reject if the polarizer does not cover the Viewing Area.</td><td>Minor</td></tr>
<tr><td>Corner Chip</td><td>Criteria for Corner Chip
t = Glass thickness
Accept If
a ≤ 1.5 mm or
b ≤ 1.5 mm
c ≤ t
  </td><td>Minor</td></tr>
<tr><td>Corner Chip</td><td>Accept If
a ≤ 3.0 mm
or
b ≤ 3.0 mm
  </td><td>Minor</td></tr>
</table>

Items	Criterion for Defects	Defect Type
Chip on contact pad	**Criteria for Chips on contact pad** t = Glass thickness Accept if b ≤ 1/3 width of contact ledge 	Minor
Chip on Face of Display	**Criteria for Chips on Face of Display** Accept if b ≤ 1.5mm 	Minor
Chip on Back of Display	**Criteria for Chips on Back of Display** Accept if b ≤ 3.0 mm 	Minor

Definition of W & L & ϕ (Unit: mm)

Note: Distance between any two defects should be over 5 mm

8. GENERAL OLED MODULE HANDLING & CARE

8.1 Mechanical Handling

8.1.1 Avoid mechanical stress, such as shock and pressure. For parts designed without bezel, exercise caution to avoid glass chipping. When handled with bare fingers, pay special attention to sharp glass edges to avoid potential injury.

8.1.2 Avoid touching Flex contact pad with bare fingers and avoid mechanical stress and pressure on the flex.

8.1.3 Handle the polarizer with care. Avoid hard or sharp objects in contact with the display surface.

8.1.4 Store and operate the OLED display within the specified ratings. It is recommended to store them as they have been contained in the inner container at the time of delivery from us.

8.1.5 Avoid corner contact to display during assembly or installation to end products.

8.1.6 Installation Bending: The flex is generally designed to facilitate mounting to a PCB or connector. It is not a dynamic flex. Therefore, bending should be limited to less than 3 times.

8.1.7 Bending Radius: The minimum bending radius is as shown in the product drawing or equal to the thickness of the rear cap glass, whichever is smaller.

8.1.8 Wipe off saliva or water drops immediately. Contact with water over a long period of time may cause damage of polarizer or color fading, while an active OLED display with water condensation on its surface will cause corrosion of metal traces.

8.1.9 Cleaning:

8.1.9.1 Particle/ Foreign materials: Use non-abrasive cloth (Recommended Smartat Cleanroom Wipes WIP-1009 D Series) to gently wipe over the surface of the display in one direction.

8.1.9.2 Glue/ Adhesive Residue:

8.1.9.2.1 Method 1: Use non-abrasive cloth (Recommended Smartat Cleanroom Wipes WIP-1009 D Series) and applicator (dipped in IPA or ethanol if necessary) to gently wipe over the surface of the display in one direction.

8.1.9.2.2 Method 2: Use the finger cot to gently clean the stain on by rubbing it on the polarizer in one direction.

8.2 ESD

8.2.1 Electrostatic discharge (ESD): OLED modules are semiconductor devices. Take ESD handling precautions by wearing a ground strap and avoid contacting electrical connections.

Condition	MM	HBM
Vdd mode	200v	2000v
Vss mode	200v	2000v
IO mode	200v	2000v