Terminal Voltage ±2.7V to ±5V, 128 Taps, Up/Down Interface

The Intersil ISL95710 is a digitally controlled potentiometer (XDCP). The device consists of a resistor array, wiper switches, a control section, and nonvolatile memory. The wiper position is controlled by a Up/Down interface.

The potentiometer is implemented by a resistor array composed of 127 resistive elements and a wiper switching network. Between each element and at either end are tap points accessible to the wiper terminal. The position of the wiper element is controlled by the $\overline{CS}$, U/$\overline{D}$, and $\overline{INC}$ inputs. The position of the wiper can be stored in nonvolatile memory and then be recalled upon a subsequent power-up operation.

The device can be used as a three-terminal potentiometer or as a two-terminal variable resistor in a wide variety of applications including:

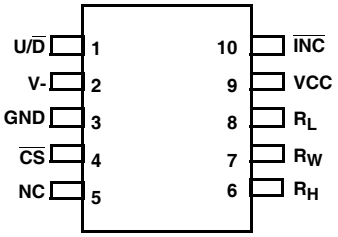
- Industrial and automotive control
- Parameter and bias adjustments
- Amplifier bias and control

Features

- Non-Volatile Solid-State Potentiometer
- Up/Down Interface with Chip Select Enable
- DCP Terminal Voltage ±2.7V to ±5.5V
- 128 Wiper Tap Points
  - Wiper position stored in nonvolatile memory and recalled on power-up
- 127 Resistive Elements
  - Typical R_{TOTAL} tempco = ±50ppm/°C
  - End to end resistance range ±20%
- Low Power CMOS
  - Standby current, 1µA
  - Active current, 3mA max
  - V_{CC} = 2.7V to 5.5V
  - V- = -2.7V to -5.5V
- High Reliability
  - Endurance, 200,000 data changes per bit
  - Register data retention, 50 years
- R_{TOTAL} Values = 10kΩ, 50kΩ
- Packages
  - 10 Ld MSOP
  - Pb-free plus anneal (RoHS compliant)

Pinout

ISL95710
(10 LD MSOP)
TOP VIEW



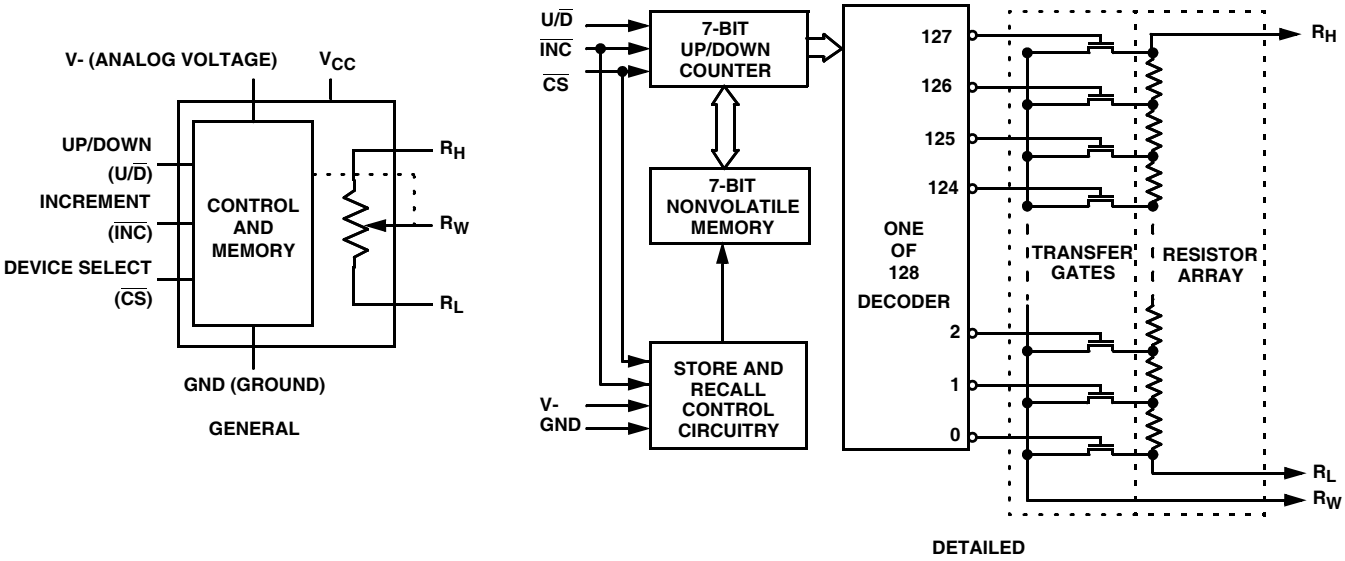
Ordering Information

PART NUMBER (Notes 1, 2)	PART MARKING	RESISTANCE OPTION (Ω)	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL95710WIU10Z	AKR	10k	-40 to +85	10 Ld MSOP	M10.118
ISL95710UIU10Z	AKP	50k	-40 to +85	10 Ld MSOP	M10.118

NOTES:

1. Add “-T” suffix for tape and reel.
2. Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Block Diagram



Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
1	U/$\overline{D}$	Controls the direction of wiper movement and whether the counter is incremented or decremented
2	V-	Negative bias voltage for the potentiometer wiper control
3	GND	Ground
4	$\overline{CS}$	Chip select. The device is selected when the $\overline{CS}$ input is LOW. Also used to initiate a nonvolatile store
5	NC	No Connect. Pin is to be left unconnected
6	R_H	A fixed terminal for one end of the potentiometer resistor
7	R_W	The wiper terminal which is equivalent to the movable terminal of a potentiometer
8	R_L	A fixed terminal for one end of the potentiometer resistor
9	VCC	Positive logic supply voltage
10	$\overline{INC}$	Increment input; negative edge triggered

Absolute Maximum Ratings

Temperature under bias . . . . . -65°C to +135°C
Storage temperature . . . . . -65°C to +150°C
Voltage on $\overline{CS}$, $\overline{INC}$, U/D and VCC
with respect to GND . . . . . -1V to +6V
Voltage on V- (referenced to GND) . . . . . -6V
$\Delta V = |V_{(RH)}-V_{(RL)}|$ 12V
Lead temperature (soldering 10 seconds) . . . . . 300°C
I_W (10 seconds) . . . . . ±6mA
ESD (Mil-Std 883, Method 3015) . . . . . >2kV
ESD Machine Model . . . . . >150V

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} (°C/W)
MSOP Package	+170

Recommended Operating Conditions

Temperature Range (Industrial) . . . . . -40°C to +85°C
V_{CC} . . . . . 2.7V to 5.5V
V- . . . . . -2.7V to -5.5V

CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device (at these or any other conditions above those listed in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE:

3. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Analog Specifications

Over recommended operating conditions unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (Note 1)	MAX	UNIT
R_{TOTAL}	R_H to R_L resistance	W option		10		kΩ
		U option		50		kΩ
	R_H to R_L resistance tolerance		-20		+20	%
TC_R (Note 12, 13)	Resistance Temperature Coefficient	I_{DCP} = 1mA T = -40°C to +85°C		±50		ppm/°C
V_{RH},V_{RL}	R_H,R_L terminal voltage		V-		V_{CC}	V
R_W	Wiper resistance	V- = -5.5V; V_{CC} = +5.5V wiper current = $(V_{CC}-V-)/R_{TOTAL}$		70	200	Ω
$C_H/C_L/C_W$ (Note 13)	Potentiometer Capacitance			10/10/25		pF
I_{LkgDCP}	Leakage on DCP pins	Voltage at pins; V- to V_{CC}	-1	0.1	1	µA
VOLTAGE DIVIDER MODE (V- @ R_L; V_{CC} @ R_H; Voltage at R_W = V_{RW} unloaded)						
INL (Note 6)	Integral non-linearity		-1		1	LSB (Note 2)
DNL (Note 5)	Differential non-linearity	W, U options	-0.5		0.5	LSB (Note 2)
ZSerror (Note 3)	Zero-scale error	W option	0	1	4	LSB (Note 2)
		U option	0	0.5	2	
FSerror (Note 4)	Full-scale error	W option	-4	-1	0	LSB (Note 2)
		U option	-2	-0.5	0	
TC_V (Notes 7, 13)	Ratiometric Temperature Coefficient	DCP Register set at 63d, T = -40°C to +85°C		±4		ppm/°C
RESISTOR MODE (Measurements between R_W and R_L with R_H not connected, or between R_W and R_H with R_L not connected)						
RINL (Note 11)	Integral non-linearity	DCP register set between 20 hex and 5F hex. Monotonic over all tap positions	-1		1	MI (Note 8)
RDNL (Note 10)	Differential non-linearity	W, U options	-0.5		0.5	MI (Note 8)
Roffset (Note 9)	Offset	DCP Register set to 00 hex, W option	0	2	5	MI (Note 8)
		DCP Register set to 00 hex, U option	0	0.5	2	

Operating Specifications

Over the recommended operating conditions unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (Note 1)	MAX	UNIT
I_{CC1}	V_{CC} supply current, volatile write/read	$\overline{CS}$ = V_{IL}, U/$\overline{D}$ = V_{IL} or V_{IH} and $\overline{INC}$ = V_{IL} or V_{IH}, R_L, R_H, R_W not connected			500	µA
I_{V-1}	V- supply current, volatile write/read	$\overline{CS}$ = V_{IL}, U/$\overline{D}$ = V_{IL} or V_{IH} and $\overline{INC}$ = V_{IL} or V_{IH}, R_L, R_H, R_W not connected	-100			µA
I_{CC2}	V_{CC} supply current, nonvolatile write	U/$\overline{D}$ = V_{IL} or V_{IH} and $\overline{INC}$ = V_{IH}, $\overline{CS}$ = transitions from V_{IL} to V_{IH}. R_L, R_H, R_W not connected			500	µA
I_{V-2}	V- supply current, nonvolatile write	U/$\overline{D}$ = V_{IL} or V_{IH} and $\overline{INC}$ = V_{IH}, $\overline{CS}$ = transitions from V_{IL} to V_{IH}. R_L, R_H, R_W not connected	-3			mA
I_{CCSB}	V_{CC} current (standby)	V_{CC} = +5.5V, I^2C Interface in Standby State			1	µA
		V_{CC} = +3.6V, I^2C Interface in Standby State			1	µA
I_{V-SB}	V- current (standby)	V- = -5.5V, $\overline{CS}$ = V_{IH}	-5			µA
		V- = -3.6V, $\overline{CS}$ = V_{IH}	-2			µA
I_{LkgDig}	Leakage current, at pins $\overline{INC}$, $\overline{CS}$, and U/$\overline{D}$	V_{IL} or V_{IH} applied at pin	-10		10	µA
$I_{IL\_\overline{CS}}$	Leakage at CS, input low	V_{IL} = 0V	-300			µA
Vpor	Power-on recall for both V- and V_{CC}	V-	-2.5			V
		V_{CC}			2.5	V
V- Ramp	V- ramp rate				-0.2	V/ms
EEPROM SPECS						
	EEPROM Endurance		200,000			Cycles
	EEPROM Retention	Temperature ≤ +75°C	50			Years
3-WIRE INTERFACE SPECS						
V_{IL}	$\overline{INC}$, $\overline{CS}$, and U/$\overline{D}$ input buffer LOW voltage		-0.3		0.3*V_{CC}	V
V_{IH}	$\overline{INC}$, $\overline{CS}$, and U/$\overline{D}$ input buffer HIGH voltage		0.7*V_{CC}		V_{CC}+ 0.3	V
Hysteresis (Note 13)	$\overline{INC}$, $\overline{CS}$, and U/$\overline{D}$ input buffer hysteresis			0.15* V_{CC}		V
Cpin	$\overline{INC}$, $\overline{CS}$, and U/$\overline{D}$ pin capacitance			10		pF

AC Electrical Specifications

V_{CC} = 5V ±10%, T_A = Full Operating Temperature Range unless otherwise stated

SYMBOL	PARAMETER	MIN	TYP (Note 1)	MAX	UNIT
t_{CI}	$\overline{CS}$ to $\overline{INC}$ setup	100			ns
t_{ID}	$\overline{INC}$ HIGH to U/$\overline{D}$ change	100			ns
t_{DI}	U/$\overline{D}$ to $\overline{INC}$ setup	1			µs
t_{IL}	$\overline{INC}$ LOW period	1			µs
t_{IH}	$\overline{INC}$ HIGH period	1			µs
t_{IC}	$\overline{INC}$ inactive to $\overline{CS}$ inactive	1			µs
t_{CPHS} (Note 14)	$\overline{CS}$ deselect time (STORE)	20			ms
t_{CPHNS}	$\overline{CS}$ deselect time (NO STORE)	1			µs

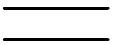
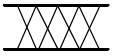
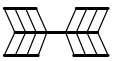
AC Electrical Specifications V_{CC} = 5V ±10%, T_A = Full Operating Temperature Range unless otherwise stated **(Continued)**

SYMBOL	PARAMETER	MIN	TYP (Note 1)	MAX	UNIT
t_{IW}	$\overline{INC}$ to R_W change		100	500	µs
t_{CYC}	$\overline{INC}$ cycle time	2			µs
t_R, t_F	$\overline{INC}$ input rise and fall time			500	µs

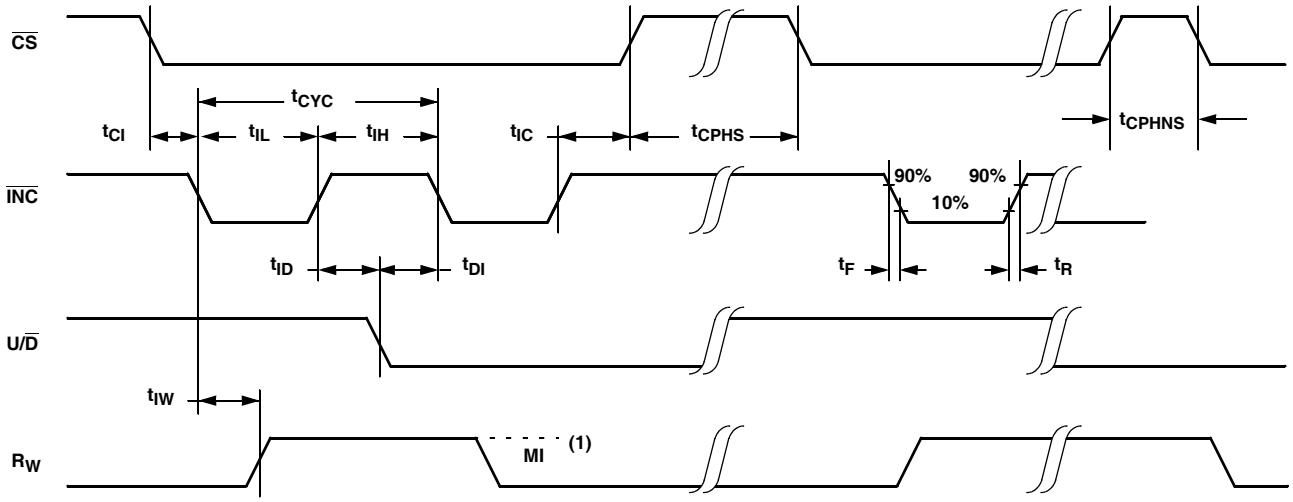
NOTES:

1. Typical values are for T_A = +25°C and 3.3V supply voltage.
2. LSB: $[V(R_W)_{127} – V(R_W)_0]/127$. $V(R_W)_{127}$ and $V(R_W)_0$ are $V(R_W)$ for the DCP register set to 7F hex and 00 hex respectively. LSB is the incremental voltage when changing from one tap to an adjacent tap.
3. ZS error = $(V(R_W)_0 – V-)/LSB$.
4. FS error = $[V(R_W)_{127} – V+]/LSB$.
5. DNL = $[V(R_W)_i – V(R_W)_{i-1}]/LSB-1$, for i = 1 to 127. i is the DCP register setting.
6. INL = $V(R_W)_i – (i • LSB – V(R_W)_0)/LSB$ for i = 1 to 127.
7. $$TC_V = \frac{Max(V(RW)_i) - Min(V(RW)_i)}{[Max(V(RW)_i) + Min(V(RW)_i)]/2} x \frac{10^6}{125°C}$$
   for i = 16 to 120 decimal. Max ( ) is the maximum value of the wiper voltage and Min ( ) is the minimum value of the wiper voltage over the temperature range.
8. MI = $|R_{127} – R_0|$ /127. R_{127} and R_0 are the measured resistances for the DCP register set to 7F hex and 00 hex respectively.
9. Roffset = R_0/MI, when measuring between RW and RL.
   Roffset = R_{127}/MI, when measuring between RW and RH.
10. RDNL = $(R_i – R_{i-1})$/MI -1, for i = 16 to 127.
11. RINL = $[R_i – (MI • i) – R_0]$/MI, for i = 16 to 127.
12. $$TC_R = \frac{[Max(Ri) - Min(Ri)]}{[Max(Ri) + Min(Ri)]/2} \times \frac{10^6}{125°C}$$
    for i = 16 to 127, T = -40°C to +85°C. Max ( ) is the maximum value of the resistance and Min ( ) is the minimum value of the resistance over the temperature range.
13. This parameter is not 100% tested.
14. t_{CPHS} is the minimum cycle time to be allowed for any non-volatile Write by the user. It is the time from a valid STORE condition to the end of the self-timed internal non-volatile write cycle. No $\overline{CS}$ or $\overline{INC}$ changes should be allowed.

Symbol Table

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

A.C. Timing



NOTE (1): MI IN THE TIMING DIAGRAM REFERS TO THE MINIMUM INCREMENTAL CHANGE IN THE WIPER POSITION.

Typical Performance Curves

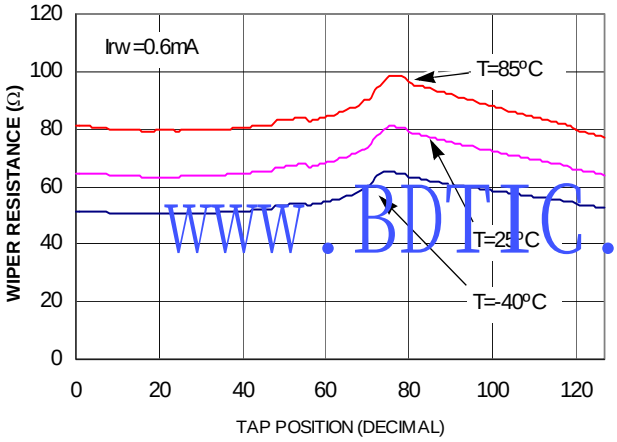


FIGURE 1. WIPER RESISTANCE vs TAP POSITION [I(RW) = V_{CC}/R_{TOTAL}] for 10kΩ (W)

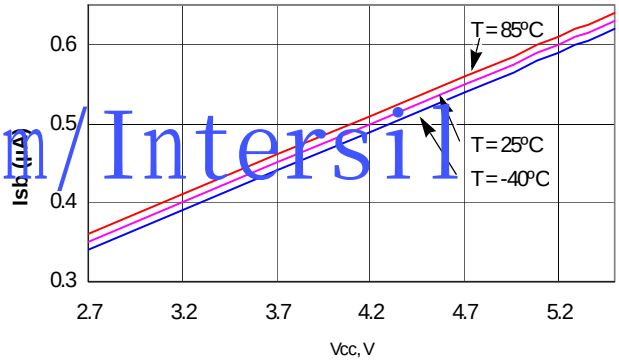


FIGURE 2. STANDBY I_{CC} vs V_{CC}

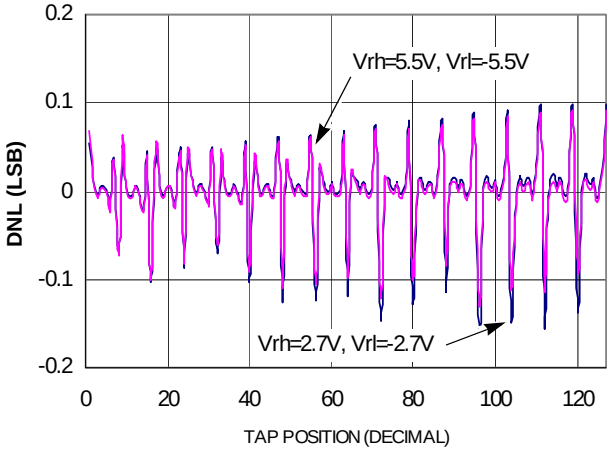


FIGURE 3. DNL vs TAP POSITION IN VOLTAGE DIVIDER MODE FOR 10kΩ (W)

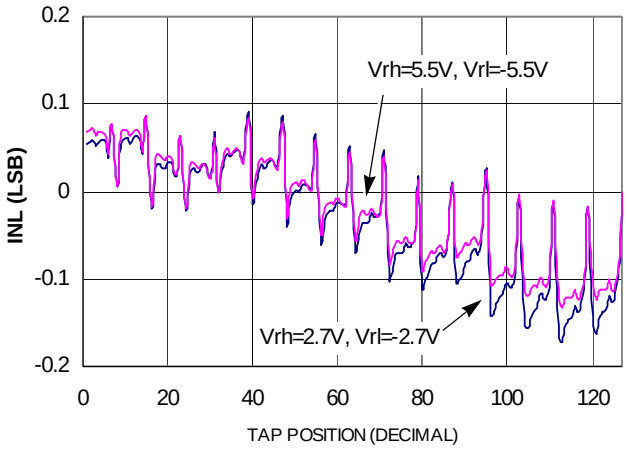


FIGURE 4. INL vs TAP POSITION IN VOLTAGE DIVIDER MODE FOR 10kΩ (W)

Typical Performance Curves (Continued)

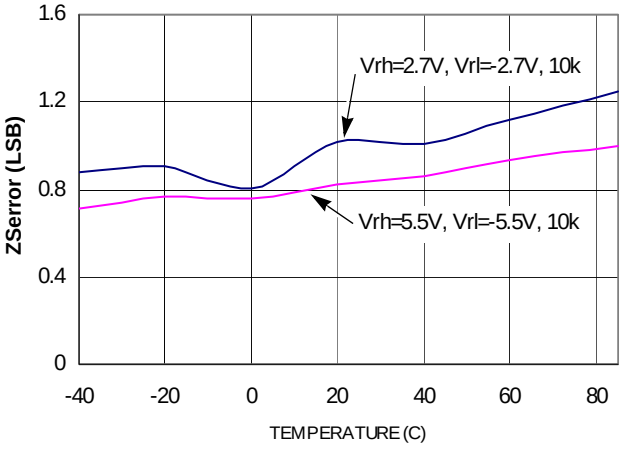


FIGURE 5. ZSerror vs TEMPERATURE

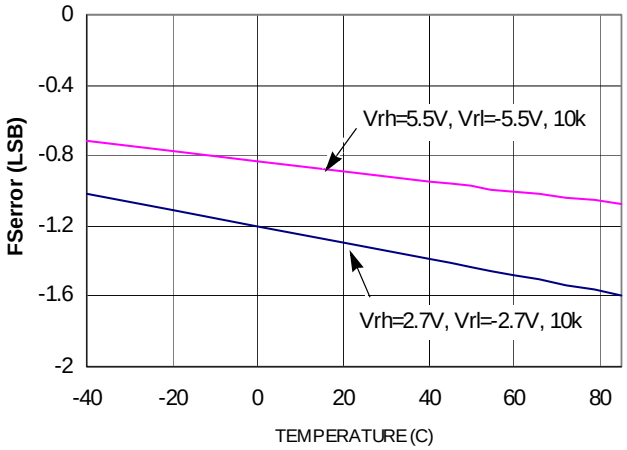


FIGURE 6. FSerror vs TEMPERATURE

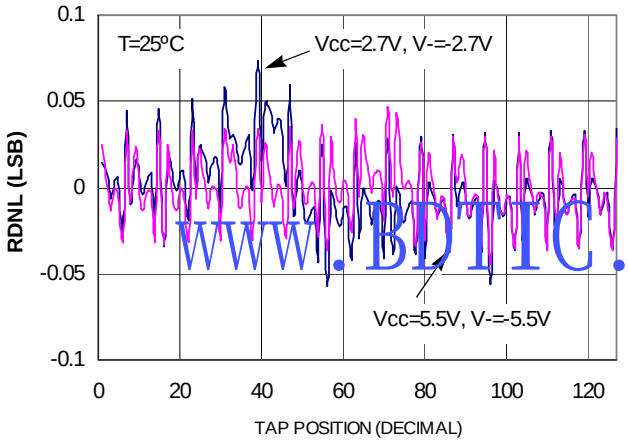


FIGURE 7. DNL vs TAP POSITION IN RHEOSTAT MODE FOR 10kΩ (W)

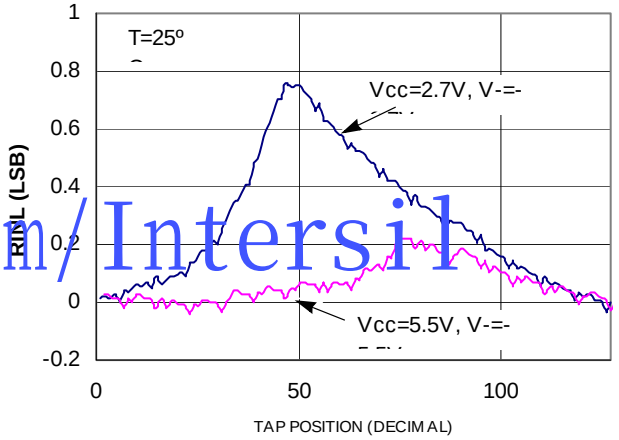


FIGURE 8. INL vs TAP POSITION IN RHEOSTAT MODE FOR 10kΩ (W)

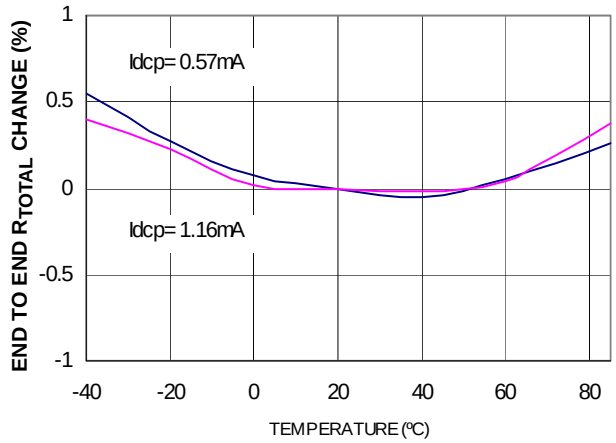


FIGURE 9. END TO END R_{TOTAL} % CHANGE vs TEMPERATURE

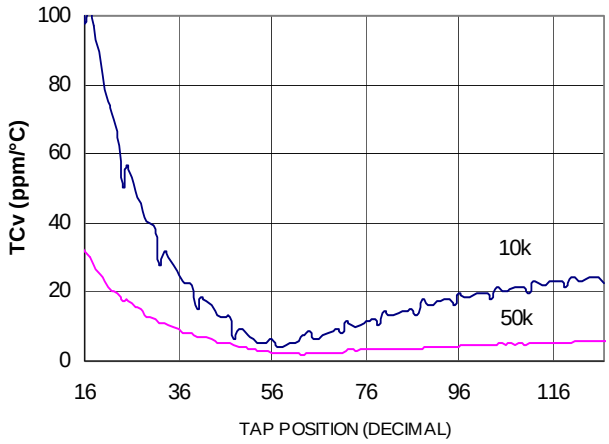


FIGURE 10. TC FOR VOLTAGE DIVIDER MODE IN ppm

Typical Performance Curves (Continued)

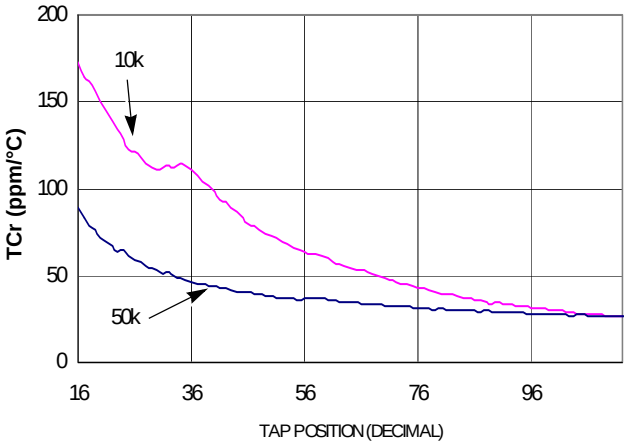


FIGURE 11. TC FOR RHEOSTAT MODE IN ppm

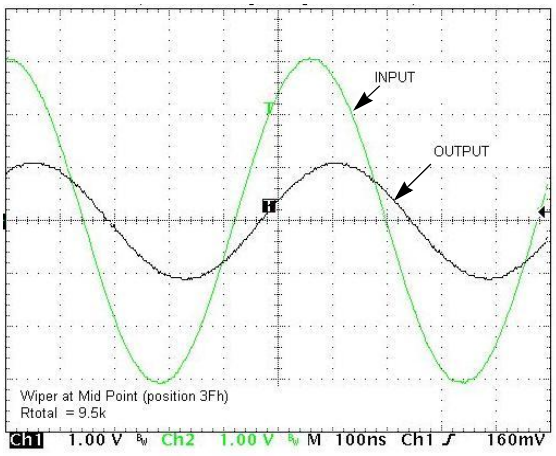


FIGURE 12. FREQUENCY RESPONSE (1.8MHz)

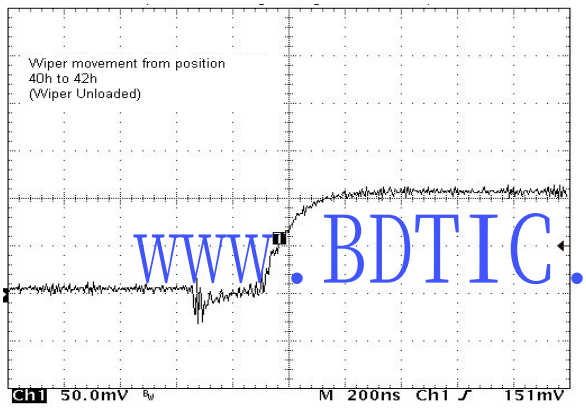


FIGURE 13. WIPER MOVEMENT

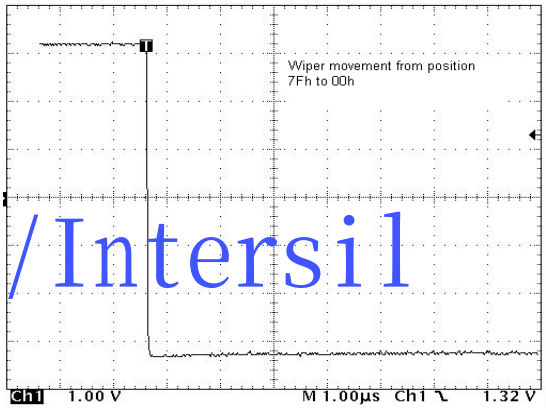


FIGURE 14. LARGE SIGNAL SETTLING TIME

Power Up and Down Requirements

In order to prevent unwanted tap position changes, or an inadvertent store, bring the $\overline{CS}$ and $\overline{INC}$ high before or concurrently with the V_{CC} pin on power-up. The potentiometer voltages must be applied after this sequence is completed. During power-up, the data sheet parameters for the DCP do not fully apply until 1ms after V_{CC} reaches its final value. The V_{CC} ramp spec is always in effect.

Pin Descriptions

R_H and R_L

The high (R_H) and low (R_L) terminals of the ISL95710 are equivalent to the fixed terminals of a mechanical potentiometer. The terminology of R_L and R_H references the relative position of the terminal in relation to wiper movement direction selected by the U/$\overline{D}$ input and not the voltage potential on the terminal.

R_W

R_W is the wiper terminal and is equivalent to the movable terminal of a mechanical potentiometer. The position of the wiper within the array is determined by the wiper counter.

Up/Down (U/$\overline{D}$)

The U/$\overline{D}$ input controls the direction of the wiper movement and whether the wiper counter is incriminated or decremented.

Increment ($\overline{INC}$)

The $\overline{INC}$ input is negative-edge triggered. Toggling $\overline{INC}$ will move the wiper and either increment or decrement the wiper counter in the direction indicated by the logic level on the U/$\overline{D}$ input.

Chip Select ($\overline{CS}$)

The device is selected when the $\overline{CS}$ input is LOW. The current wiper counter value is stored in nonvolatile memory when $\overline{CS}$ is returned HIGH while the $\overline{INC}$ input is also HIGH. After the store operation is complete the ISL95710 will be

placed in the low power standby mode until the device is selected once again.

Principles of Operation

There are three sections of the ISL95710: the input control, wiper counter and decode section; the nonvolatile memory; and the resistor array. The input control section operates as an up/down counter. The output of this wiper counter is decoded to turn on a electronic switch connecting a point on the resistor array to the wiper output. The contents of the wiper counter can be stored in nonvolatile memory and retained for future use. The resistor array is comprised of individual resistors connected in series. At either end of the array and between each resistor is an electronic switch that transfers the potential at that point to the wiper.

The wiper, when at either fixed terminal, acts like its mechanical equivalent and does not move beyond the last position. The wiper counter does not wrap around when clocked to either extreme.

The electronic switches on the device operate in a “make before break” mode when the wiper changes tap positions. If the wiper is moved several positions, multiple taps are connected to the wiper for t_{IW} ($\overline{INC}$ to R_W change). The R_{TOTAL} value for the device can temporarily be reduced by a significant amount if the wiper is moved several positions.

When the device is powered-down, the last wiper position stored will be maintained in the nonvolatile memory. When power is restored, the contents of the memory are recalled and the wiper is set to the value last stored.

Instructions and Programming

The $\overline{INC}$, U/$\overline{D}$ and $\overline{CS}$ inputs control the movement of the wiper along the resistor array. With $\overline{CS}$ set LOW the device is selected and enabled to respond to the U/$\overline{D}$ and $\overline{INC}$ inputs. HIGH to LOW transitions on $\overline{INC}$ will increment or decrement (depending on the state of the U/$\overline{D}$ input) a seven bit wiper counter. The output of this wiper counter is decoded to select one of 128 wiper positions along the resistive array.

The value of the wiper counter is stored in nonvolatile memory whenever $\overline{CS}$ transitions HIGH while the $\overline{INC}$ input is also HIGH.

The system may select the ISL95710, move the wiper and deselect the device without having to store the latest wiper position in nonvolatile memory. After the wiper movement is performed as described above and once the new position is reached, the system must keep $\overline{INC}$ LOW while taking $\overline{CS}$ HIGH. The new wiper position will be maintained until changed by the system or until a power-up/down cycle recalls the previously stored data.

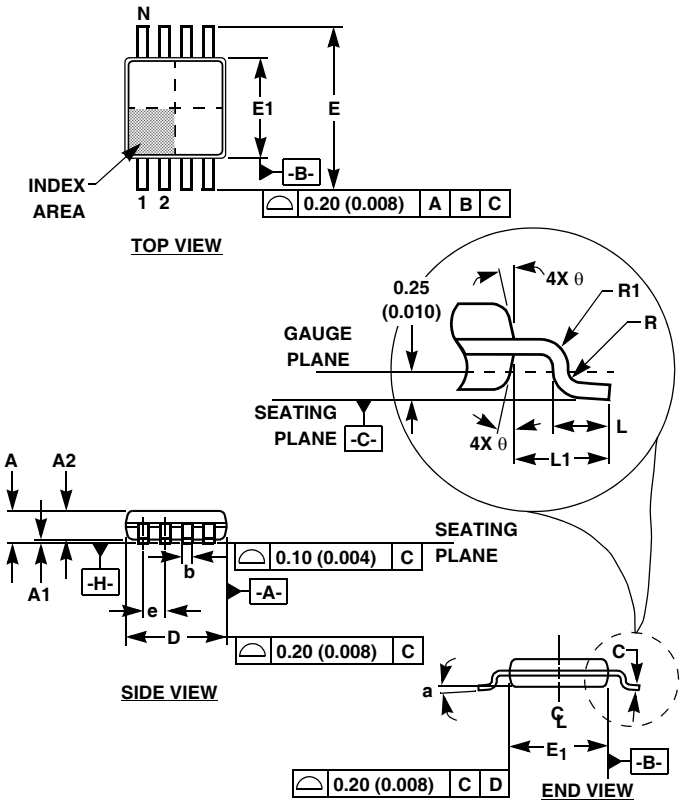
This procedure allows the system to always power-up to a preset value stored in nonvolatile memory; then during system operation minor adjustments could be made. The adjustments might be based on user preference, system parameter changes due to temperature drift, etc.

The state of U/$\overline{D}$ may be changed while $\overline{CS}$ remains LOW. This allows the host system to enable the device and then move the wiper up and down until the proper trim is attained. During initial power-up $\overline{CS}$ must go high along with or before V_{CC} to avoid an accidental store generation.

TABLE 1. MODE SELECTION

$\overline{CS}$	$\overline{INC}$	U/$\overline{D}$	MODE
L	↘	H	Wiper up
L	↘	L	Wiper down
↗	H	X	Store wiper position
H	X	X	Standby current
↗	L	X	No store, return to standby
H	H	X	Standby
↘	L	H	Wiper up one position (not recommended)
↘	L	L	Wiper down one position (not recommended)

Mini Small Outline Plastic Packages (MSOP)



M10.118 (JEDEC MO-187BA)

10 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.037	0.043	0.94	1.10	-
A1	0.002	0.006	0.05	0.15	-
A2	0.030	0.037	0.75	0.95	-
b	0.007	0.011	0.18	0.27	9
c	0.004	0.008	0.09	0.20	-
D	0.116	0.120	2.95	3.05	3
E1	0.116	0.120	2.95	3.05	4
e	0.020 BSC		0.50 BSC		-
E	0.187	0.199	4.75	5.05	-
L	0.016	0.028	0.40	0.70	6
L1	0.037 REF		0.95 REF		-
N	10		10		7
R	0.003	-	0.07	-	-
R1	0.003	-	0.07	-	-
θ	5^o	15^o	5^o	15^o	-
α	0^o	6^o	0^o	6^o	-

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NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-187BA.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. Dimension “D” does not include mold flash, protrusions or gate burrs and are measured at Datum Plane. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions and are measured at Datum Plane. [- H -] Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. Formed leads shall be planar with respect to one another within 0.10mm (.004) at seating Plane.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Datums [-A -] and [- B -] to be determined at Datum plane [- H -].
11. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems.
Intersil Corporation’s quality certifications can be viewed at www.intersil.com/design/quality