ISL6225 Dual PWM Controller Provides Complete DDR Memory Power System Solution

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Introduction

As computer memory bandwidth is pushed further and further to multi-Gb/s levels, new memory technologies are emerging. The DDR (Dual Data Rate) memory is an evolutionary step on this path that along with increased data rate maintains the low cost legacy of SDRAMs and thus will dominate most PC markets for several years to come [1]. The DDR memory not only increases the memory bandwidth but also reduces memory power consumption. The major contributors to reduced power consumption are lower operating voltage, lower signal voltage swing associated with SSTL_2 logic, and reduced time spent in an active mode. All these features make DDR memory a desirable component for mobile, battery-powered applications [2, 3].

DDR Memory Power Requirements

The new memory comes with some additional requirements. The increased bandwidth made available by SSTL_2 signaling require special clock techniques, proper layout, a power source tracking reference signal, and line termination.

The important part of SSTL_2 signaling is that bus signals are referenced to the reference voltage VREF that is usually held symmetrically between VDDQ and VSS. It is important that VREF stays symmetrically positioned between VDDQ and VSS levels over variations in environmental and supply parameters, Figure 1. The termination voltage VTT should be within ±40mV of VREF. The VDDQ voltage, currently 2.5V nominal value, should have ±200mV tolerance.

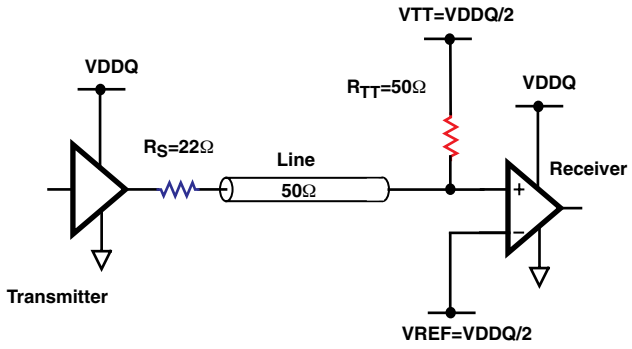


FIGURE 1. DDR MEMORY TERMINATION

Each terminated line consumes 16.2 mA. With about 125 lines compliant with SSTL_2 specifications, this theoretically makes maximum current capability of VTT supply Imax=2.025A, sourcing or sinking. In reality, the front bus is operating on frequency of 100MHz, 133MHz and any given memory state is actively present on the bus for a very short moment of time of several tens of nanoseconds as DDR memory operates with a double rate. Practically, the VTT current gets dramatically averaged in output capacitors due to a low duty factor (~15 to 30%) of read-write states [4]. The terminating VTT power supply requirements depend only on the number of lines and value of the terminating resistors used and does not vary with memory size. Measurements done in practical circuits show typical current levels in a range of 0.5A. Tests show that the more memory is engaged by the software, the lower is VTT current. All these suggests that the same optimized solution can be used for various computer applications.

The VDDQ power supply usually provides current not only to the memory banks, but to a 'north bridge' controller and some other circuitry as well. The current has a permanent base level in a range of 2.0–3.0A. The base level depends on how aggressive the power management scheme of a memory controller isand also varies with memory size. The bigger memory draws more current on background. Depending on the computing task performed, the current can peak up to 4.0A.

ISL6225–Provides Complete Power Solution for DDR Memory

The ISL6225 dual switcher accomplishes all of the goals associated with DDR memory power by combining two synchronous PWM voltage regulators into a single IC. Its unique design allows the IC to both source and sink current on one of the channels. This ability allows the IC to be adapted very effectively to a DDR memory power solution when the DDR pin is set high.

The first PWM channel is used to regulate 2.5VDC (V_{DDQ})in a typical "buck" regulator fashion. The output voltage of the first channel is set to the required VDDQ level by the external voltage divider. This makes the chip compatible not only with current DDR memory specifications, but, also, with future DDR II requirements. To provide the required tracking function, the output of this regulated voltage is divided down to 1.25VDC by an external R/R divider and fed back into the IC as a tracking reference voltage.The reference voltage VREF required by the DDR memory chips is provided via the PG2/REF pin that can source up to 10mA. This output also serves as a reference for the VTT channel. The second channel will then regulate to 1.25VDC (V_{TT}) with high precision.

Please refer to the ISL6225 datasheet, FN9049, for more information [5].

Quick Start Evaluation

Out Of The Box

The ISL6225EVAL1 comes in a “ready-to-test” state. The board comes equipped with several jumpers pre-populated for battery operation. Use Table 1, which describes jumper function, for test setup. Table 2 illustrates the input and output voltage and current specifications.

NOTE: Note: This Application Note is for the DDR solution only.

Required Test Equipment

To fully test the ISL6225 chip functionality characterized by this Application Note, the follow equipment is needed:

- 4 channel oscilloscope with probes
- 2 electronic loads
- 2 bench power supplies
- precision digital multi-meters
- Digital pulse generator

TABLE 1. JUMPER FUNCTIONALITY

Jumper #	State	Function
JP1	POP	Normal Operation
	NOP	Measure operating current I_{VCC}
JP2	POS1	Enable hysteretic operation
	POS2	FCCM mode
JP3	POP	Connect EN1 to VCC
	NOP	External EN1
JP4	POP	Connect EN2 to VCC
	NOP	External EN2
JP5	POS1	Operate in Battery Mode
	POS2	Operate in 5V Mode

Power Connections

With the all supplies turned OFF, connect the 0-24V power supply positive terminal to the VIN post (J2) on the EVAL board and the negative terminal to the nearest GND post (J3). Then connect the 0-5V power supply positive terminal to the VCC post (J4) and the negative terminal to the nearest GND post (J1)

It should be noted that VIN must be powered up prior to VCC in all cases.

TABLE 2. INPUT/OUTPUT VOLTAGE/CURRENT OPERATING SPECIFICATIONS.

	VIN	VCC	VDDQ	VTT
Voltage	5-24V	5V	2.5V	1.25V
Imax	3A	3A	6A	3A
Inom	-	-	3A	2A

Load Connections

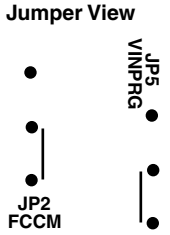
Connect the first electronic load positive terminal to VDDQ (J5) and the negative terminal to GND (J6). Connect the positive terminal of the second electronic load to VTT (J6) and negative terminal to the nearest GND post (J9).

Performance Characterization

This section will show measured performance data from a standard bench setup. It will include descriptions of each experiment performed and how to recreate them.

NOTES:

- Jumper JP1 should be populated.
- Connect JP2 in FCCM mode
- Connect JP5 in the EN5V position.
- VIN = 5V, VCC = 5V.



Modes of Operation

Figure 10 shows a typical circuit for One-Step Conversion. This is accomplished by populating jumper JP5 in POS1. In this arrangement, V_{DDQ} is converted directly from the battery voltage. V_{TT} is then converted directly from the V_{DDQ} output. This setup has the advantage of not requiring a regulated system voltage to supply the power train.

Two-Step Conversion is also available on the ISL6225 DDR evaluation board. This approach requires a regulated 5 volt system rail to provide power to the converters. The V_{DDQ} converter takes the system rail voltage while the V_{TT} converter is cascaded from V_{DDQ}. In this case, V_{IN} must be tied to GND through a 100kOhm resistor. This is done by populating jumper JP5 in POS2 and tying the V_{CC} and V_{IN} terminals together on the application board.

Soft-Start

In a start up event, the IC is required to ramp both output voltages smoothly to their programmed level. To do this, the chip must disable the undervoltage and pgood circuitry until the output has risen to within 75% of its target. Only then is PGOOD released and the part allowed to operate normally.

With $I_{VDDQ} = I_{VTT} = 3A$, the start up event is captured in Figure 2.

- Connect the digital pulse generator to JP3 and JP4 to allow for external enabling of the chip.
- Set the scope to trigger on EN (J12).

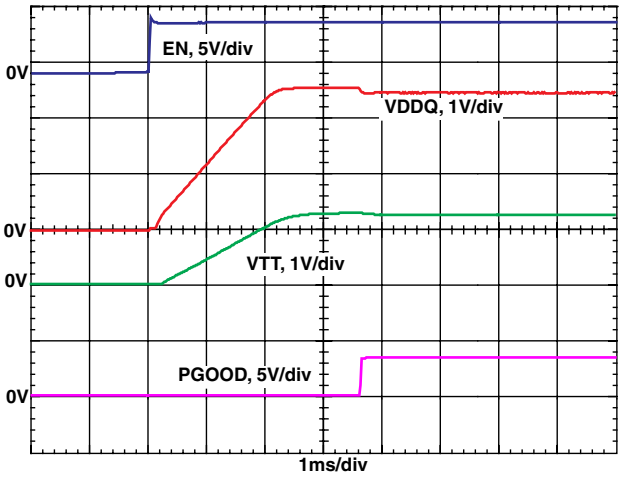


FIGURE 2. INITIAL START UP

Steady-State Operation

Under normal operating conditions, the ISL6225 should regulate 2.5V and 1.25V with minimal effort and output voltage ripple. Figure 3 illustrates converter waveforms during normal operating conditions.

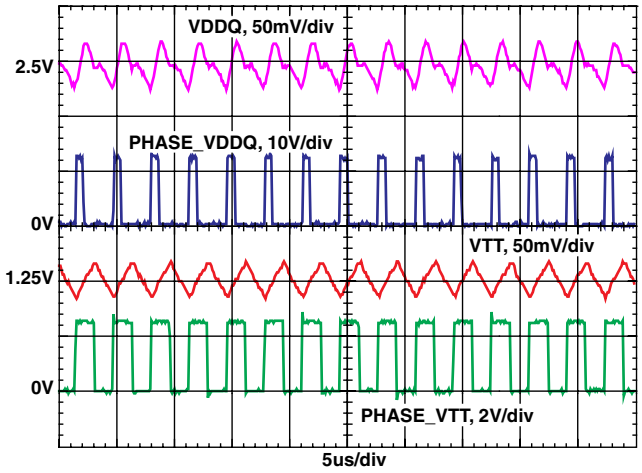


FIGURE 3. NORMAL OPERATION

Transient Response

The ISL6225 in DDR applications is required to handle load transients of 0-3A on V_{TT}. For these tests, there is a static load of 3A from V_{DDQ} to GND.

Sourcing Mode (V_{TT} to GND)

The output voltage excursion under a load transient event is shown in Figure 4. The load swings 0-3A from V_{TT}.

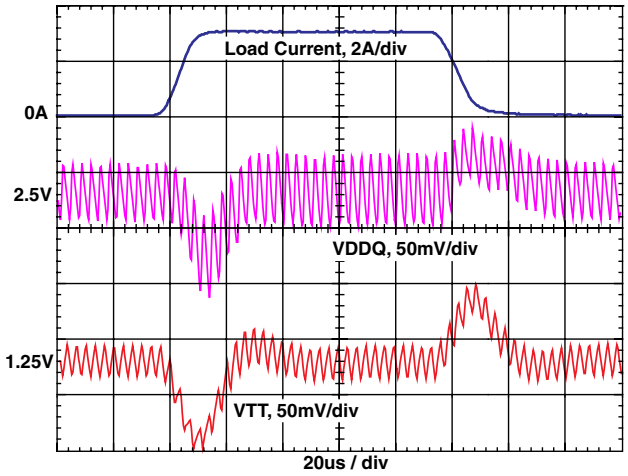


FIGURE 4. LOAD TRANSIENT (VTT - GND)

Sinking Mode (V_{DDQ} to V_{TT})

The output voltage excursion under a load transient in sinking mode is shown in Figure 5. The load swings 0-3A from V_{DDQ} into V_{TT}. Reconfigure the second electronic load between V_{DDQ} and V_{TT} for this experiment.

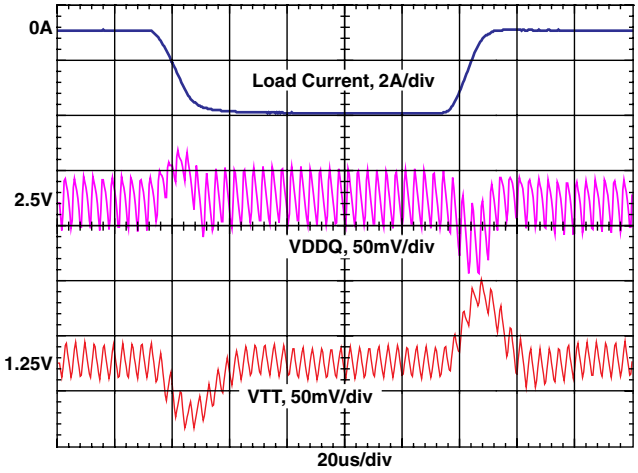


FIGURE 5. LOAD TRANSIENT (VDDQ - VTT)

Efficiency

It is important to illustrate that each channel of the ISL6225 is highly efficient, which contributes to an overall high system efficiency. Figures 6...9 demonstrate all perspectives of efficiency for the ISL6225 in DDR mode.

NOTE:

- Measure voltage at board terminals
- Allow thermal equilibrium
- TA = 25C
- No forced air

Individual channel efficiency for V_{TT} is captured for both sinking and sourcing current in Figure 6 and Figure 7 respectively.

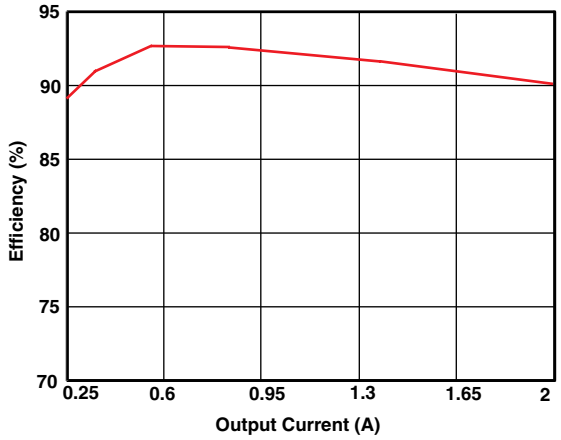


FIGURE 6. VTT EFFICIENCY. SOURCING MODE

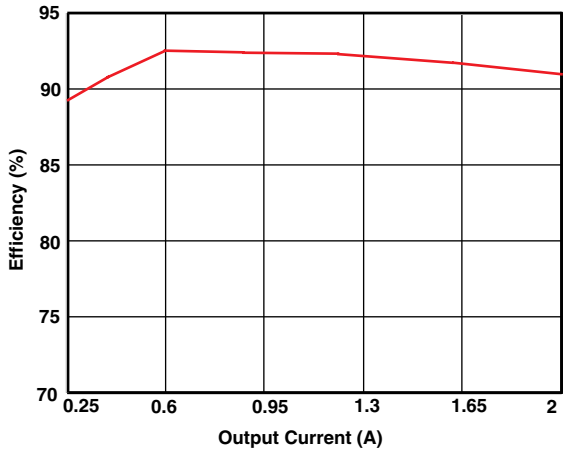


FIGURE 7. VTT EFFICIENCY. SINKING MODE

The individual channel efficiency for V_{DDQ} is illustrated in Figure 8. Both V_{TT} and V_{DDQ} provide efficiency greater than 90% for nearly all loading conditions.

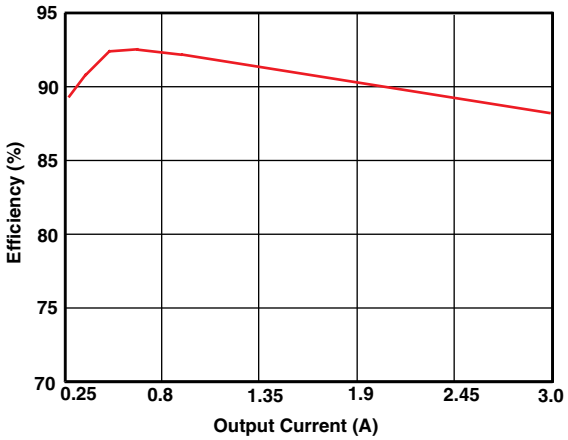


FIGURE 8. VDDQ EFFICIENCY

Overall efficiency for the ISL6225 in DDR mode can be seen in Figure 9.

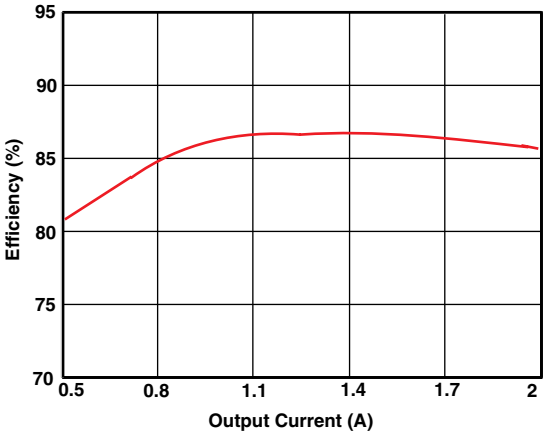


FIGURE 9. OVERALL EFFICIENCY

References

1. JEDEC STANDARD JESD8-9A. Stub Series Terminated Logic for 2.5V (SSTL_2)

2. L.L. Wang, P. Leung, F. Tabrizi, ‘DDR DRAMs Pare Down Power for Laptops’, Portable Design, July 2000

3. V. Muratov, S. Wiktor, J. Li, ‘Powering DDR Memory -- Mysteries and Realities’, PCIM -- HFPC 2001, pp. 11-18

4. J. Janzen, ‘Calculating Memory System Power for DDR SDRAM,’ Micron Application Note, 2001

5. ISL6225 Data Sheet, Intersil Corporation, File No. FN9049

Intersil documents are available on the web at http://www.intersil.com.

ISL6225 EVAL1 Schematic

The evaluation board schematic is shown in Figure 10. The board allows evaluation of ISL6225 performance for DDR memory using either single-step or dual-step power conversion schemes. The recommended Bill of Materials (BOM) is presented in Table 3.

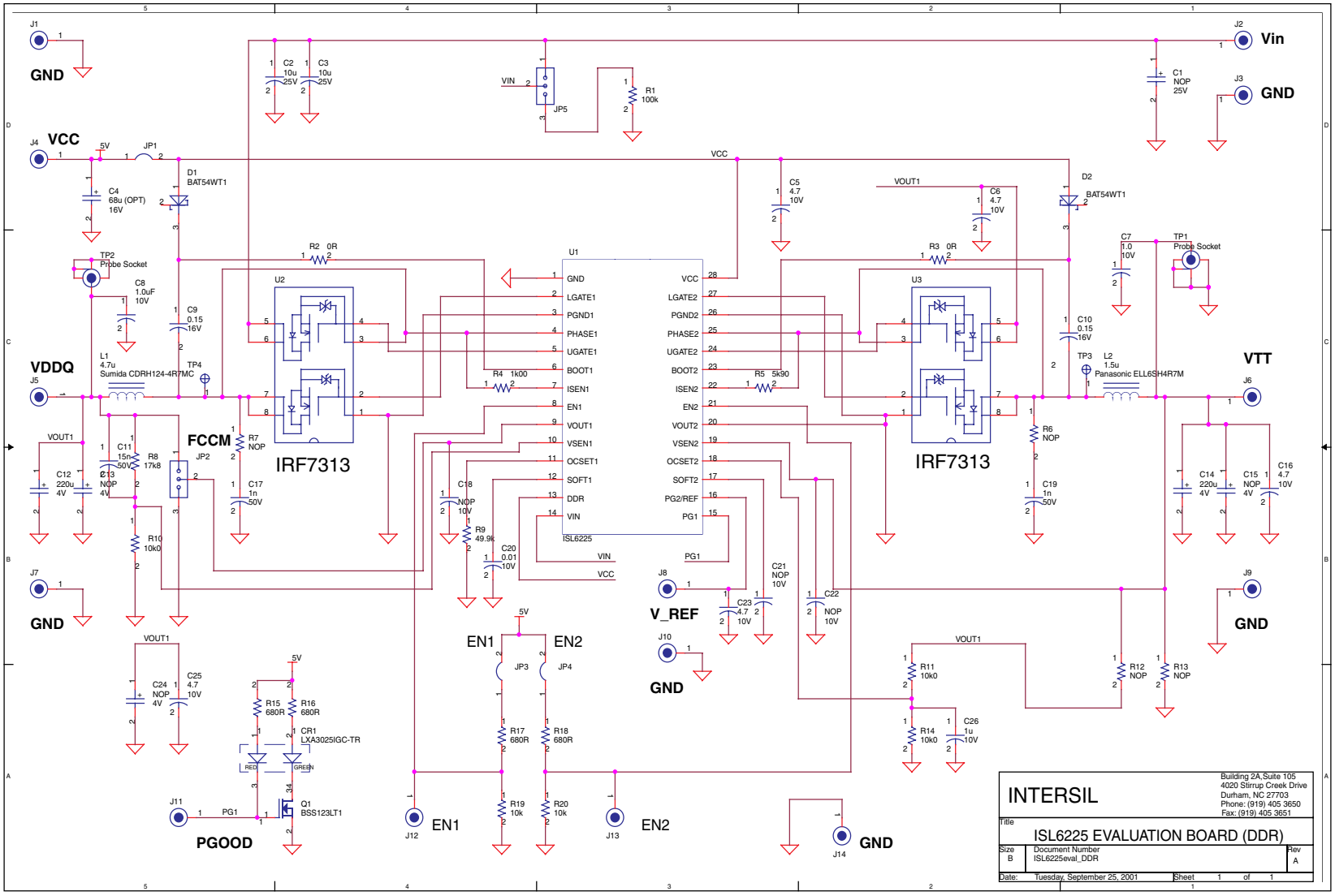


FIGURE 10. APPLICATION BOARD SCHEMATIC

Bill of Materials

TABLE 3. BILL OF MATERIALS

Qty	Reference	Description	Package	Vendor	Part No.
1	CR1	LED			LXA3025IGC-TR
1	C1	NOP		Sanyo	OSCON 25SP56M
2	C2, C3	10uF		Tayo Yuden	TMK432BJ106KM
1	C4	68uF (OPT)		KEMET	T494D686(1)016AS
5	C5, C6, C16, C23, C25	4.7uF		Tayo Yuden	LMK316BJ475ML
3	C18, C21, C22	NOP		KEMET	C1206C105K8RAC
2	C7, C8	1.0uF		KEMET	C1206C105K8RAC
2	C10, C9	150nF		KEMET	C0805C154K4RAC
1	C11	15nF		KEMET	C0805C102K5RAC
2	C17, C19	1.0nF		KEMET	C0805C102K5RAC
2	C12, C14	220uF		Sanyo	4TPB220ML
1	C20	0.01uF		KEMET	C0805C103K4RAC
1	C26	10nF		KEMET	C0805C103K4RAC
3	C13, C15, C24	NOP		Sanyo	TPB330ML
2	D1, D2	Diode		Motorola	BAT54WT1
3	JP1, JP3, JP4	2-Terminal Jumper		Berg	header# 68000-236 shunt# 71363-102
2	JP2, JP5	3-Terminal Jumper		Berg	header# 68000-236 shunt# 71363-102
14	J1, J2, J3, J4, J5, J6, J7, J8, J9, J10, J11, J12, J13, J14	Binding Post		Keystone	1502TL-2
1	L1	4.7uH		Sumida	CDRH124-4R7MC
1	L2	1.5uH		Panasonic	ELL6SH1R5M
1	Q1	NMOS Transistor			BSS123LT1
2	R1	100kΩ			
2	R2, R3	0Ω			
2	R4	1.00kΩ			
2	R5	5.90kΩ			
4	R6, R7, R12, R13	NOP			
1	R8	17.8kΩ			
1	R9	49.9kΩ			
3	R10, R11, R14	10kΩ			
4	R15, R16, R17, R18	680Ω			
2	R19, R20	10kΩ			
2	TP1, TP2	Probe Socket			
2	TP3, TP4	Probe Socket			
1	U1	Power Controller IC	28-Ld SSOP	Intersil Corp.	ISL6225
2	U2, U3	Dual Bridged NMOS FETs			IRF7313

ISL6225EVAL1 Layout

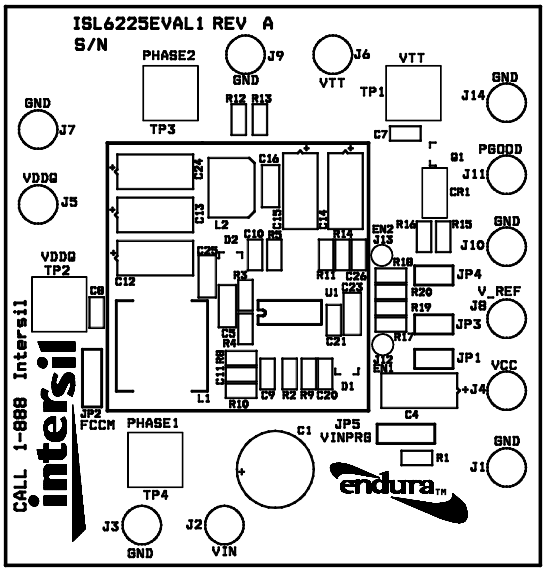


FIGURE 11. SILKSCREEN TOP

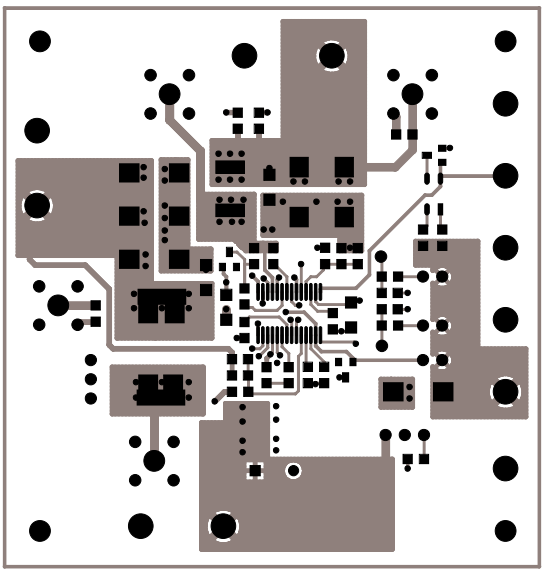


FIGURE 12. TOP LAYER

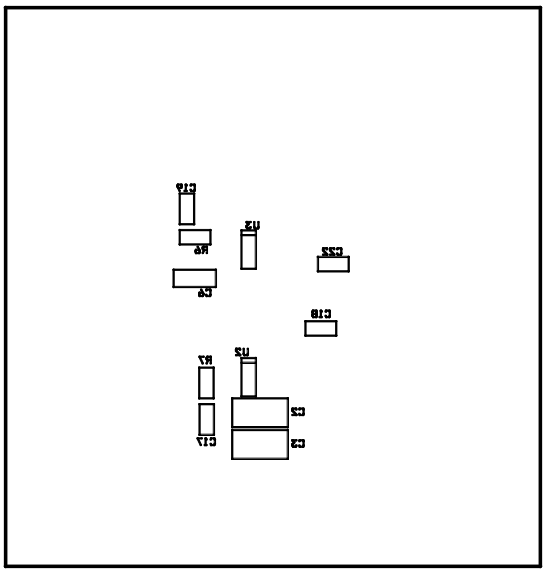


FIGURE 13. SILKSCREEN BOTTOM

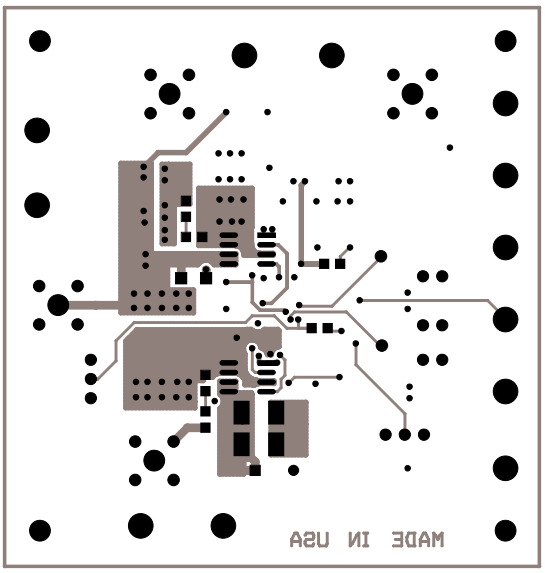


FIGURE 14. BOTTOM LAYER

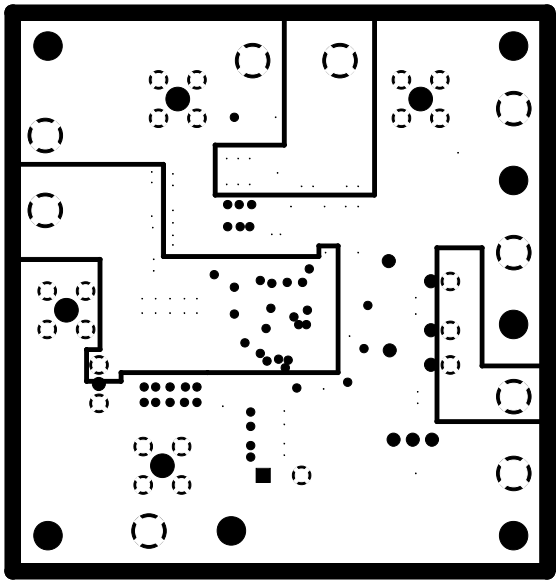


FIGURE 15. POWER INTERNAL

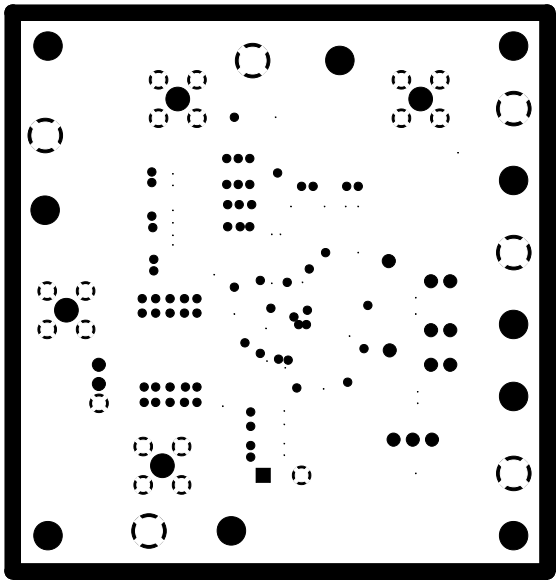


FIGURE 16. GROUND INTERNAL

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