Data Sheet | March 26, 2007 | FN7014.5

Differential DSL Line Driver

The EL1508 is designed for driving full rate ADSL signals in both CO and CPE applications at very low power dissipation. The high drive capability of 450mA makes this driver ideal for both CAP and DMT designs. It contains two wideband, high-voltage, current mode feedback amplifiers with a number of power dissipation reduction features.

These drivers achieve an MTPR distortion measurement of better than 70dB, while consuming typically 6mA of total supply current. This supply current can be set using a resistor on the I_{ADJ} pin. Two other pins (C_0 and C_1) can also be used to adjust supply current to one of four pre-set modes (full-I_S, 2/3-I_S, 1/3-I_S, and full power-down). The EL1508 operates on ±5V to ±12V supplies and retains its bandwidth and linearity over the complete supply range.

The device is supplied in a thermally-enhanced 20 Ld SOIC (0.300”), a thermally-enhanced 16 Ld SOIC (0.150”), and the small footprint (4x5mm) 24 Ld QFN packages. The EL1508 is specified for operation over the full -40°C to +85°C temperature range.

Features

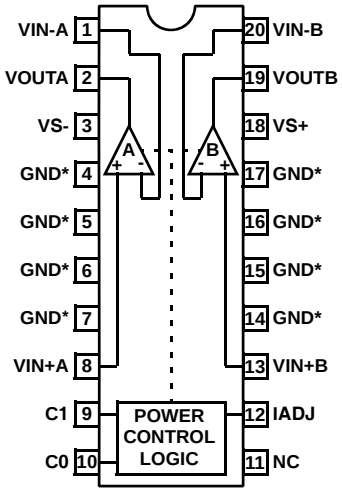
- 450mA output drive capability
- 43.6V_{P-P} differential output drive into 100Ω
- $2^{nd}/3^{rd}$ harmonics of -85dBc/-75dBc
- MTPR of -70dB
- Operates down to 3mA per amplifier supply current
- Power control features
- Pin-compatible with EL1503
- Pb-free plus anneal available (RoHS compliant)

Applications

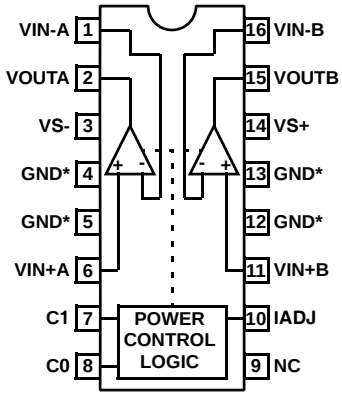
- ADSL line driver
- HDSL line driver
- Video distribution amplifier
- Video twisted-pair line driver

Pinouts

EL1508
[20 LD SOIC (0.300”)]
TOP VIEW

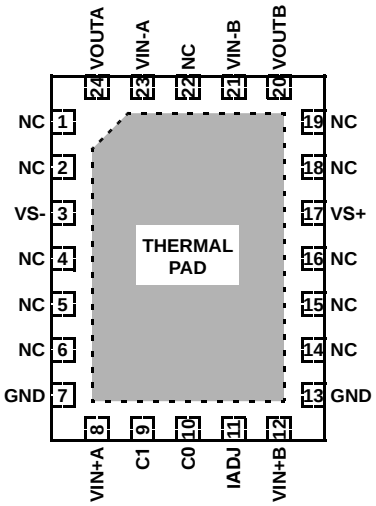


EL1508
[16 LD SOIC (0.150”)]
TOP VIEW



*GND PINS ARE HEAT SPREADERS

EL1508
(24 LD QFN)
TOP VIEW



Ordering Information

PART NUMBER	PART MARKING	TAPE & REEL	PACKAGE	PKG. DWG. #
EL1508CS	EL1508CS	-	16 Ld SOIC (0.150”)	MDP0027
EL1508CS-T7	EL1508CS	7”	16 Ld SOIC (0.150”)	MDP0027
EL1508CS-T13	EL1508CS	13”	16 Ld SOIC (0.150”)	MDP0027
EL1508CSZ (See Note)	EL1508CSZ	-	16 Ld SOIC (0.150”) (Pb-Free)	MDP0027
EL1508CSZ-T7 (See Note)	EL1508CSZ	7”	16 Ld SOIC (0.150”) (Pb-Free)	MDP0027
EL1508CSZ-T13 (See Note)	EL1508CSZ	13”	16 Ld SOIC (0.150”) (Pb-Free)	MDP0027
EL1508CM	EL1508CM	-	20 Ld SOIC (0.300”)	MDP0027
EL1508CM-T13	EL1508CM	13”	20 Ld SOIC (0.300”)	MDP0027
EL1508CMZ (See Note)	EL1508CMZ	-	20 Ld SOIC (0.300”) (Pb-Free)	MDP0027
EL1508CMZ-T13 (See Note)	EL1508CMZ	13”	20 Ld SOIC (0.300”) (Pb-Free)	MDP0027
EL1508CL	1508CL	-	24 Ld QFN	MDP0046
EL1508CL-T7	1508CL	7”	24 Ld QFN	MDP0046
EL1508CL-T13	1508CL	13”	24 Ld QFN	MDP0046
EL1508CLZ (See Note)	1508CLZ	-	24 Ld QFN (Pb-Free)	MDP0046
EL1508CLZ-T7 (See Note)	1508CLZ	7”	24 Ld QFN (Pb-Free)	MDP0046
EL1508CLZ-T13 (See Note)	1508CLZ	13”	24 Ld QFN (Pb-Free)	MDP0046

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Maximum Ratings (T_A = 25°C)

V_S+ to V_S- Supply Voltage. . . . . -0.3V to 28V
V_S+ Voltage to Ground . . . . . -0.3V to 28V
V_S- Voltage to Ground . . . . . -28V to 0.3V
Driver V_{IN}+ Voltage . . . . . V_S- to V_S+
C_0, C_1 Voltage to GND . . . . . -0.3V to 6V
I_{ADJ} Voltage to GND . . . . . -0.3V to 4V

Current into any Input 8mA
Output Current from Driver (Static) 100mA
Operating Temperature Range . . . . . -40°C to +85°C
Storage Temperature Range . . . . . -60°C to +150°C
Operating Junction Temperature . . . . . -40°C to +150°C
Power Dissipation . . . . . See Curves

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

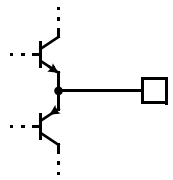
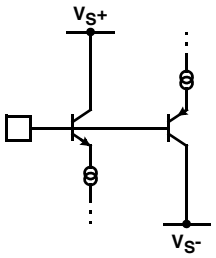
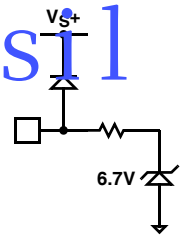
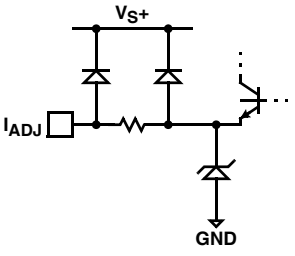
V_S = ±12V, R_F = 2.2kΩ, R_L= 65Ω, I_{ADJL} = C_0 = C_1 = 0V, T_A = 25°C. Amplifiers tested separately.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CHARACTERISTICS						
I_S+ (Full I_S)	Positive Supply Current per Amplifier	All outputs at 0V, C_0 = C_1 = 0V	10	14.5	18	mA
I_S- (Full I_S)	Negative Supply Current per Amplifier	All outputs at 0V, C_0 = C_1 = 0V	-9.5	-13.5	-17.5	mA
I_S+ (2/3 I_S)	Positive Supply Current per Amplifier	All outputs at 0V, C_0 = 5V, C_1 = 0V	7	10	12.5	mA
I_S- (2/3 I_S)	Negative Supply Current per Amplifier	All outputs at 0V, C_0 = 5V, C_1 = 0V	-6	-9	-12	mA
I_S+ (1/3 I_S)	Positive Supply Current per Amplifier	All outputs at 0V, C_0 = 0V, C_1 = 5V	3.75	5.25	7	mA
I_S- (1/3 I_S)	Negative Supply Current per Amplifier	All outputs at 0V, C_0 = 0V, C_1 = 5V	-2.75	-4.25	-6	mA
I_S+ (6.8k)	Positive Supply Current per Amplifier	All outputs at 0V, C_0 = C_1 = 0V, R_{ADJ} = 6.8k	3	3.75	4.5	mA
I_S- (6.8k)	Negative Supply Current per Amplifier	All outputs at 0V, C_0 = C_1 = 0V, R_{ADJ} = 6.8k	-3.75	-2.9	-2.25	mA
I_S+ (Power-down)	Positive Supply Current per Amplifier	All outputs at 0V, C_0 = C_1 = 5V	0.75	1.2	2	mA
I_S- (Power-down)	Negative Supply Current per Amplifier	All outputs at 0V, C_0 = C_1 = 5V	0	-0.25	-2	mA
I_{GND}	GND Supply Current per Amplifier	All outputs at 0V		1		mA
INPUT CHARACTERISTICS						
V_{OS}	Input Offset Voltage		-10	1	10	mV
ΔV_{OS}	V_{OS} Mismatch		-5	0	5	mV
I_B+	Non-Inverting Input Bias Current		-15		15	µA
I_B-	Inverting Input Bias Current		-50		50	µA
ΔI_B-	I_B- Mismatch		-25	0	25	µA
R_{OL}	Transimpedance		1.1	2.9	5	MΩ
e_N	Input Noise Voltage			3.5		nV/√Hz
i_N	-Input Noise Current			13		pA/√Hz
V_{IH}	Input High Voltage	C_0 and C_1 inputs	2.25			V
V_{IL}	Input Low Voltage	C_0 and C_1 inputs			0.8	V
I_{IH1}	Input High Current for C_1	C_1 = 5V	1	2	6	µA
I_{IH0}	Input High Current for C_0	C_0 = 5V	0.5	1	3	µA
I_{IL}	Input Low Current for C_0 or C_1	C_0 = 0V, C_1 = 0V	-1		1	µA

Electrical Specifications V_S = ±12V, R_F = 2.2kΩ, R_L= 65Ω, I_{ADJL} = C_0 = C_1 = 0V, T_A = 25°C. Amplifiers tested separately. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT CHARACTERISTICS						
V_{OUT}	Loaded Output Swing	R_L = 100Ω	±10.6	±10.8	±11.5	V
		R_L = 25Ω	±9.8	±10.2	±10.6	V
I_{OL}	Linear Output Current	A_V = 5, R_L = 10Ω, f = 100kHz, THD = -60dBc		450		mA
I_{OUT}	Output Current	V_{OUT} = 1V, R_L = 1Ω		1		A
DYNAMIC PERFORMANCE						
BW	-3 dB Bandwidth	A_V = +5		80		MHz
HD2	2nd Harmonic Distortion	f_C = 1MHz, R_L = 100Ω, V_{OUT} = $2V_{P-P}$		-90		dBc
		f_C = 1MHz, R_L = 25Ω, V_{OUT} = $2V_{P-P}$		-80		dBc
HD3	3rd Harmonic Distortion	f_C = 1MHz, R_L = 100Ω, V_{OUT} = $2V_{P-P}$		-90		dBc
		f_C = 1MHz, R_L = 25Ω, V_{OUT} = $2V_{P-P}$		-75		dBc
MTPR	Multi-Tone Power Ratio	26kHz to 1.1MHz, R_{LINE} = 100Ω, P_{LINE} = 20.4dBM		-70		dBc
SR	Slewrate	V_{OUT} from -8V to +8V measured at ±4V	450	600	800	V/µs

Pin Descriptions

16 Ld SOIC (0.150")	20 Ld SOIC (0.300")	24 Ld QFN	PIN NAME	FUNCTION	CIRCUIT
1	1	23	VIN-A	Channel A Inverting Input	 CIRCUIT 1
2	2	24	VOUTA	Channel A Output	(Reference Circuit 1)
3	3	3	VS-	Negative Supply	
4, 5	4, 5, 6, 7	7	GND	Ground Connection	
6	8	8	VIN+A	Channel A Non-inverting Input	 CIRCUIT 2
7	9	9	C1	Current Control Bit 1	 CIRCUIT 3
8	10	10	C0	Current Control Bit 2	(Reference Circuit 3)
9	11	1, 2, 4, 5, 6, 14, 15, 16, 18, 19, 22	NC	Not Connected	
10	12	11	IADJ	Supply Current Control Pin	 CIRCUIT 4
11	13	12	VIN+B	Channel B Non-inverting Input	(Reference Circuit 2)
12, 13	14, 15, 16, 17	13	GND	Ground Connection	
14	18	17	VS+	Positive Supply	
15	19	20	VOUTB	Channel B Output	(Reference Circuit 1)
16	20	21	VIN-B	Channel B Inverting Input	(Reference Circuit 1)

Typical Performance Curves

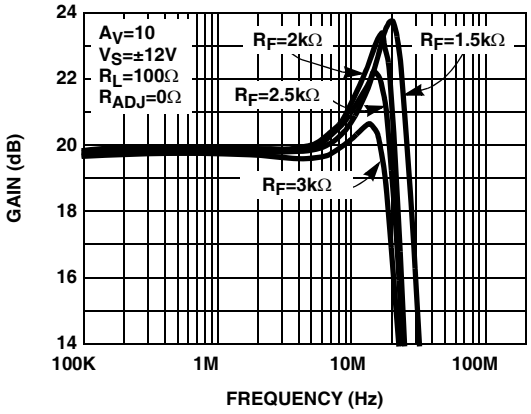


FIGURE 1. DIFFERENTIAL FREQUENCY RESPONSE vs R_F (1/3 POWER MODE)

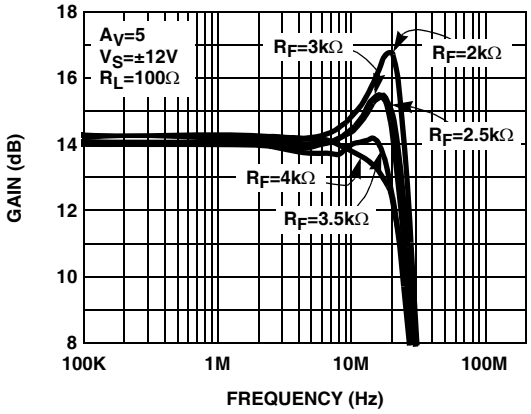


FIGURE 2. DIFFERENTIAL FREQUENCY RESPONSE (1/3 POWER MODE)

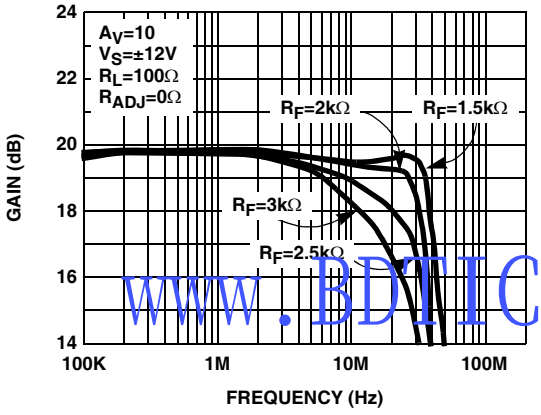


FIGURE 3. DIFFERENTIAL FREQUENCY RESPONSE vs R_F (2/3 POWER MODE)

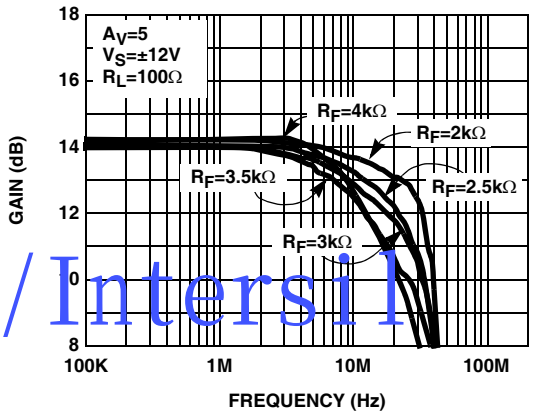


FIGURE 4. DIFFERENTIAL FREQUENCY RESPONSE (2/3 POWER MODE)

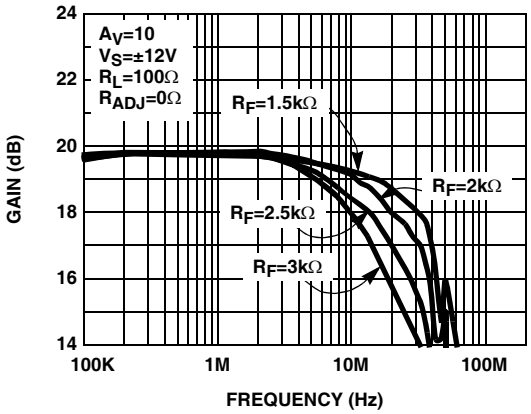


FIGURE 5. DIFFERENTIAL FREQUENCY RESPONSE vs R_F (FULL POWER MODE)

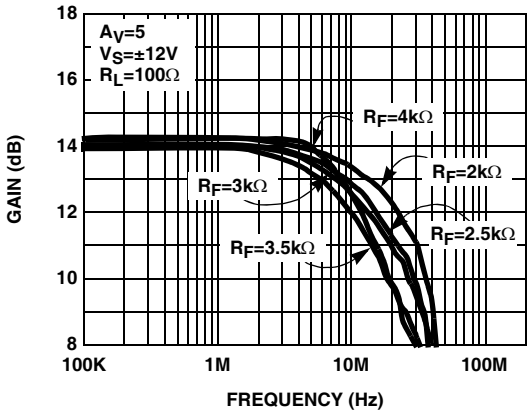


FIGURE 6. DIFFERENTIAL FREQUENCY RESPONSE (FULL POWER MODE)

Typical Performance Curves (Continued)

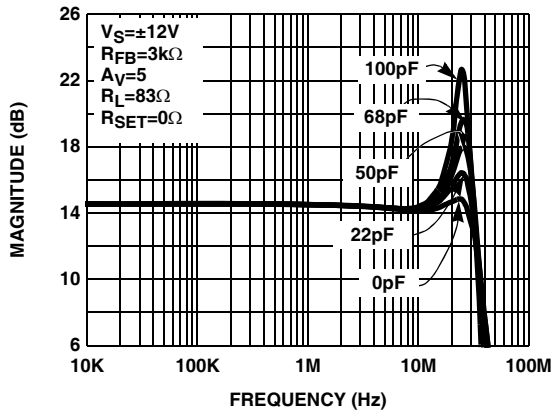


FIGURE 7. EL1508CM SINGLE-ENDED CONFIGURATION FREQUENCY RESPONSE vs C_L (1/3 POWER MODE)

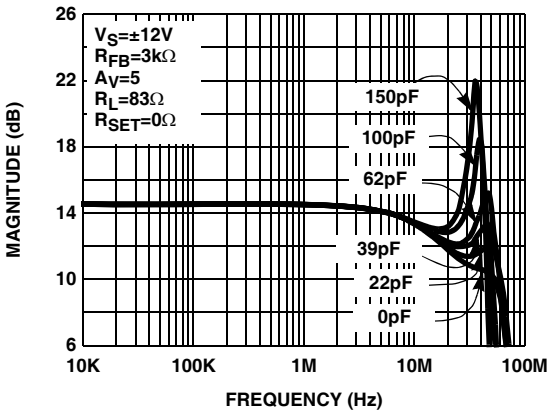


FIGURE 8. EL1508CM SINGLE-ENDED CONFIGURATION FREQUENCY RESPONSE vs C_L (1/3 POWER MODE)

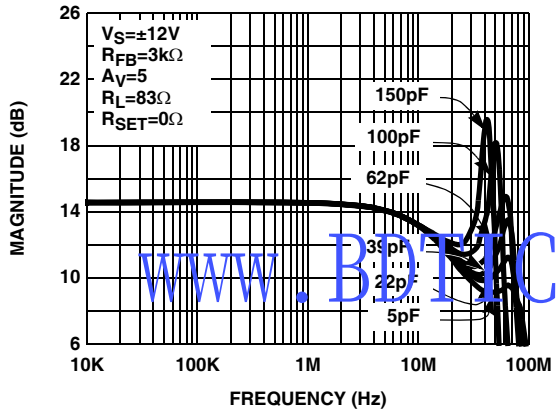


FIGURE 9. EL1508CM SINGLE-ENDED CONFIGURATION FREQUENCY RESPONSE vs C_L

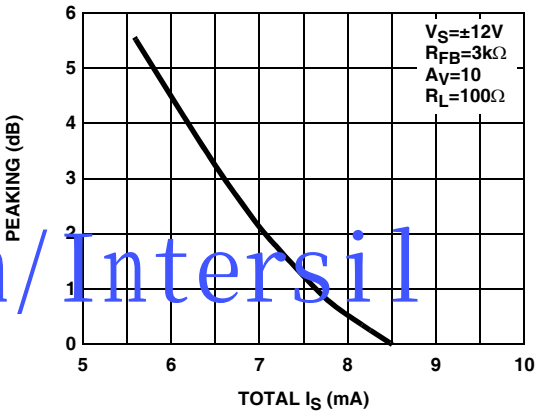


FIGURE 10. PEAKING vs I_S+

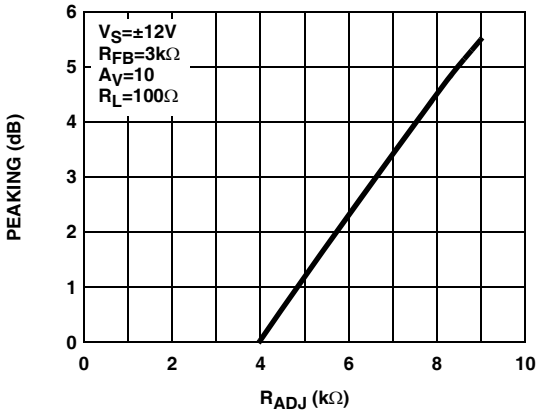


FIGURE 11. PEAKING vs R_{ADJ}

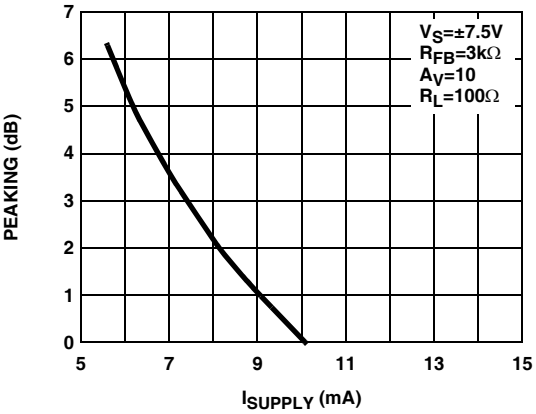


FIGURE 12. PEAKING vs I_S+

Typical Performance Curves (Continued)

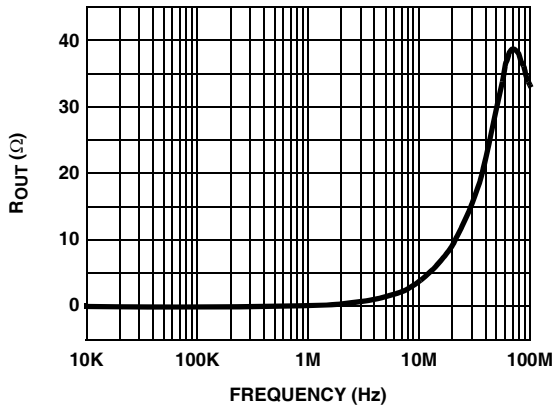


FIGURE 13. OUTPUT IMPEDANCE

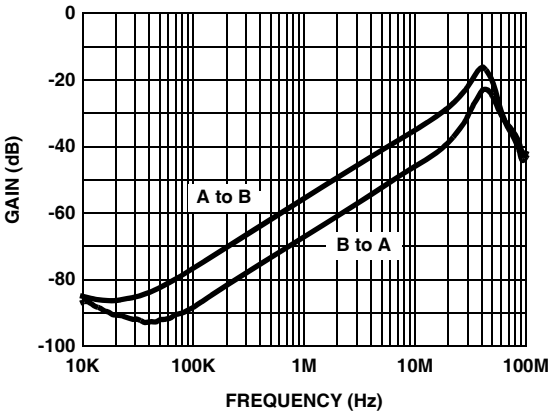


FIGURE 14. CHANCHANNEL SEPARATION

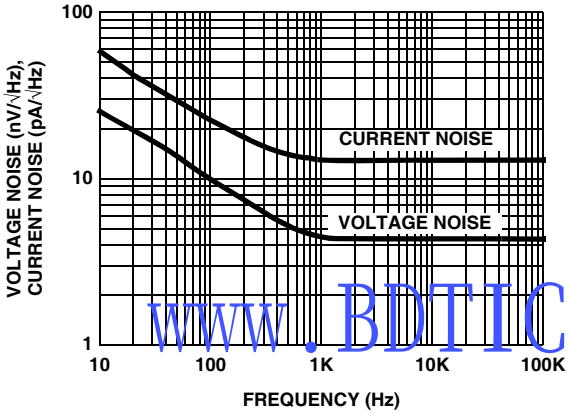


FIGURE 15. VOLTAGE AND CURRENT NOISE vs FREQUENCY

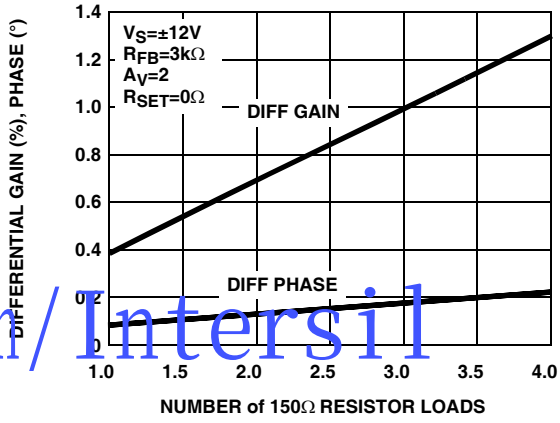


FIGURE 16. DIFFERENTIAL GAIN/PHASE, F_O=3.58MHz (2/3 POWER MODE)

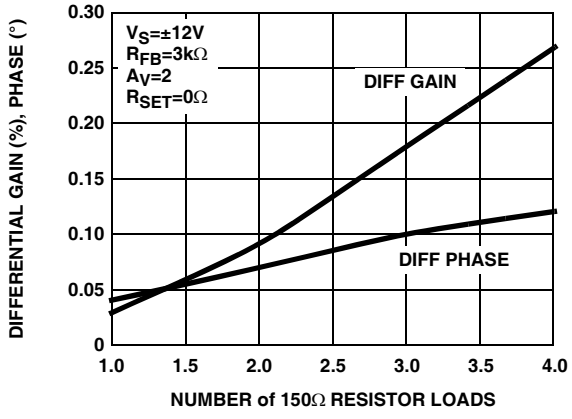


FIGURE 17. DIFFERENTIAL GAIN/PHASE, F_O=3.58MHz (2/3 POWER MODE)

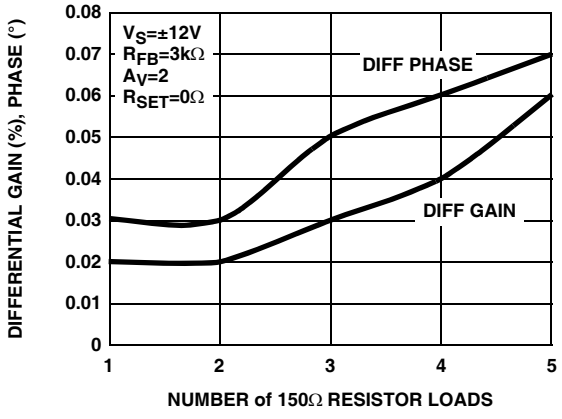


FIGURE 18. DIFFERENTIAL GAIN/PHASE, F_O=3.58MHz (FULL POWER MODE)

Typical Performance Curves - 24 Ld QFN Package

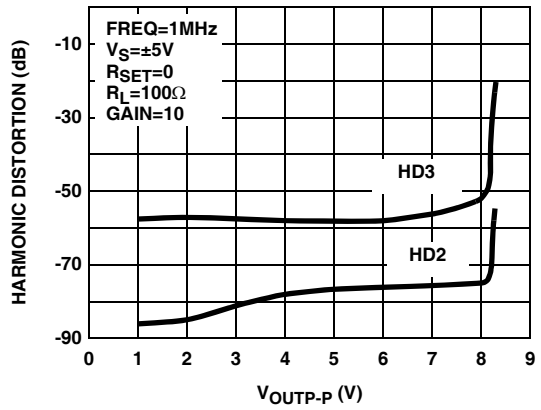


FIGURE 19. HARMONIC DISTORTION TEST (1/3 POWER MODE)

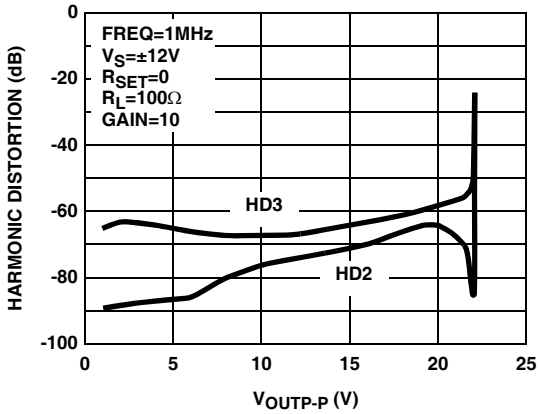


FIGURE 20. HARMONIC DISTORTION TEST (1/3 POWER MODE)

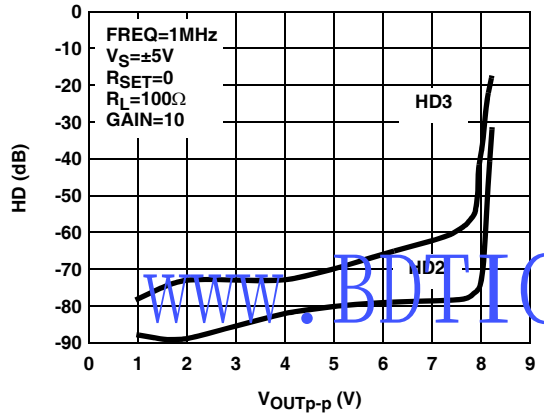


FIGURE 21. HARMONIC DISTORTION TEST (2/3 POWER MODE)

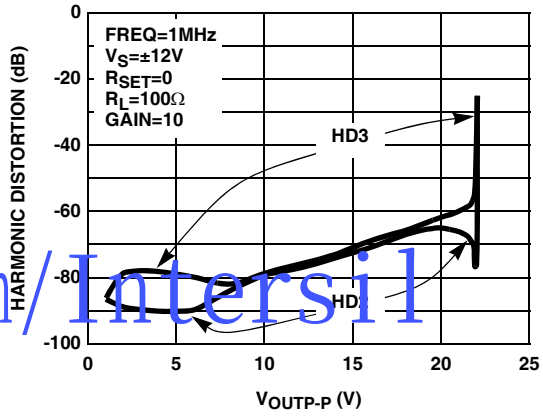


FIGURE 22. HARMONIC DISTORTION TEST (2/3 POWER MODE)

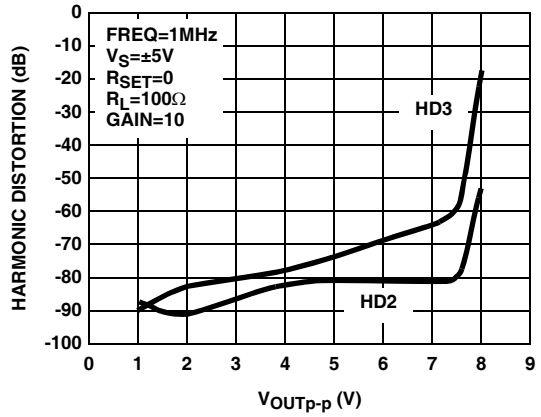


FIGURE 23. HARMONIC DISTORTION TEST (FULL POWER MODE)

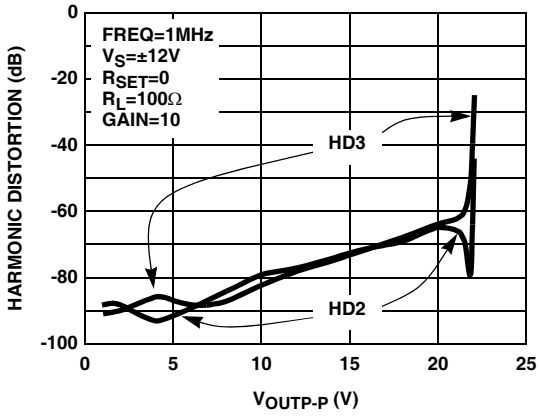


FIGURE 24. HARMONIC DISTORTION TEST (FULL POWER MODE)

Typical Performance Curves - 20 Ld SOIC (0.300") Package

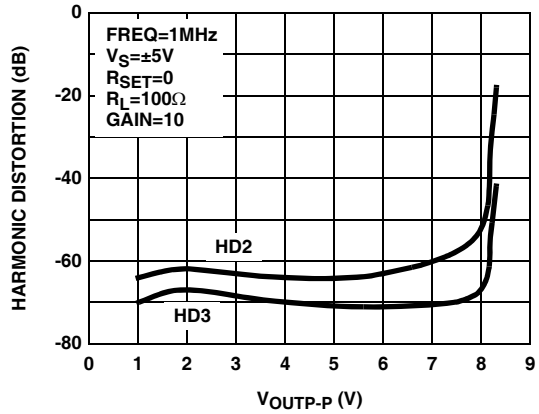


FIGURE 25. HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT VOLTAGE (1/3 POWER MODE)

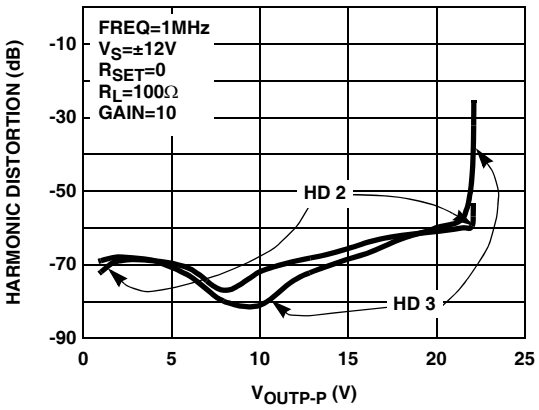


FIGURE 26. HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT VOLTAGE (1/3 POWER MODE)

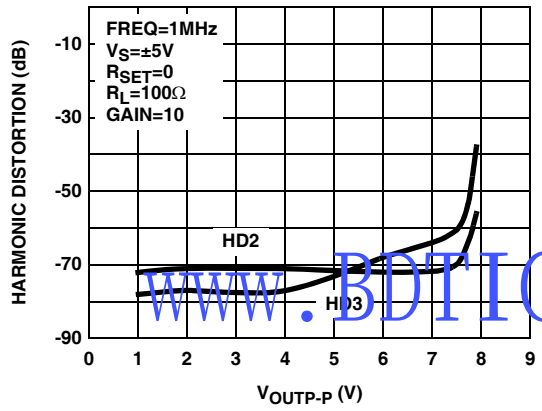


FIGURE 27. HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT VOLTAGE (2/3 POWER MODE)

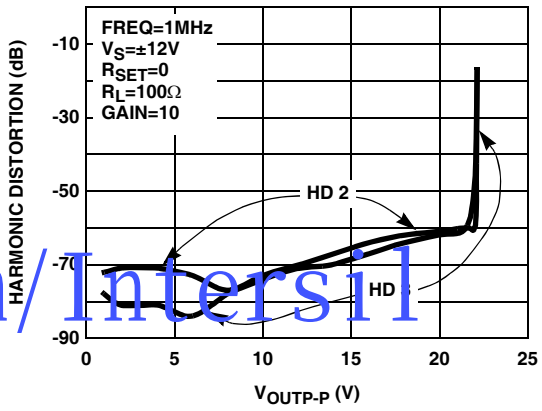


FIGURE 28. HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT VOLTAGE (2/3 POWER MODE)

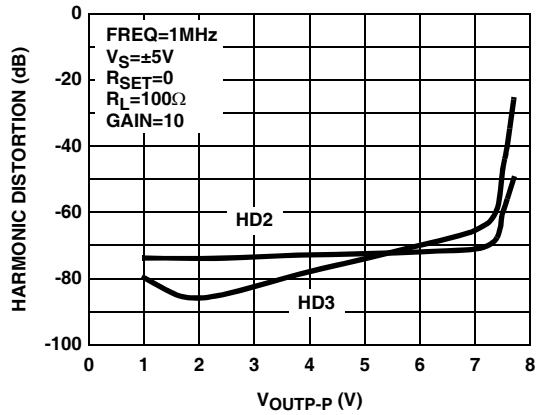


FIGURE 29. HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT VOLTAGE (FULL POWER MODE)

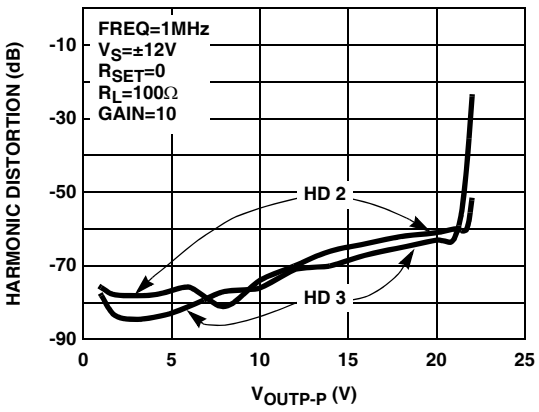


FIGURE 30. HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT VOLTAGE (FULL POWER MODE)

Typical Performance Curves

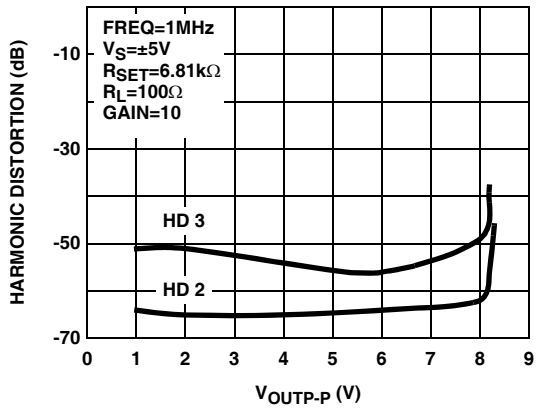


FIGURE 31. EL1508CM HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT VOLTAGE (FULL POWER MODE)

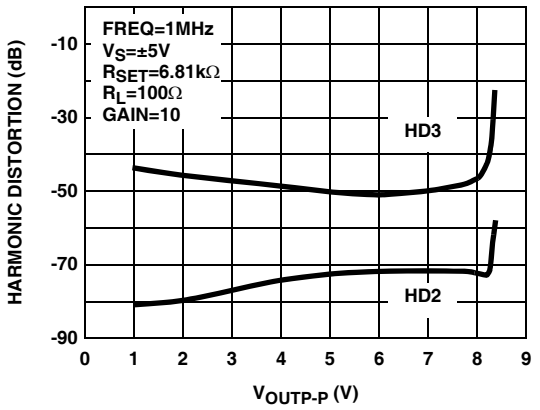


FIGURE 32. EL1508CL HARMONIC DISTORTION TEST (FULL POWER MODE)

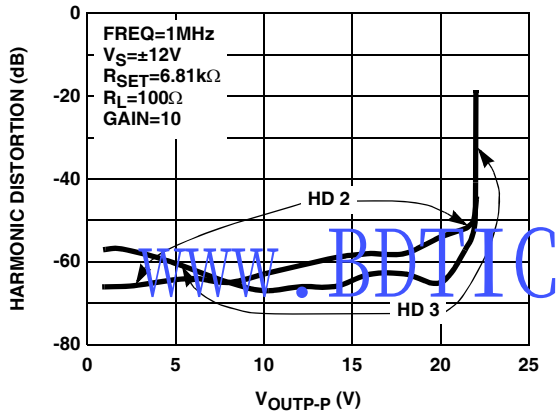


FIGURE 33. EL1508CM HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT VOLTAGE (FULL POWER MODE)

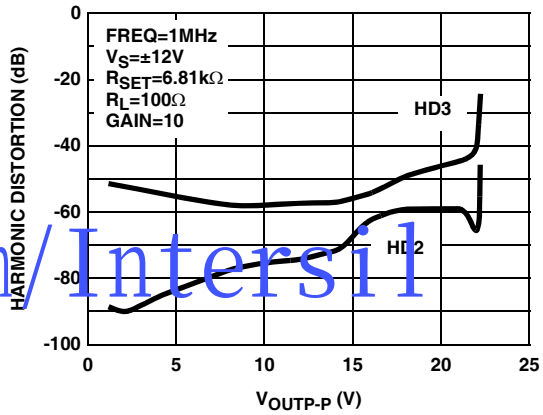


FIGURE 34. EL1508CL HARMONIC DISTORTION TEST (FULL POWER MODE)

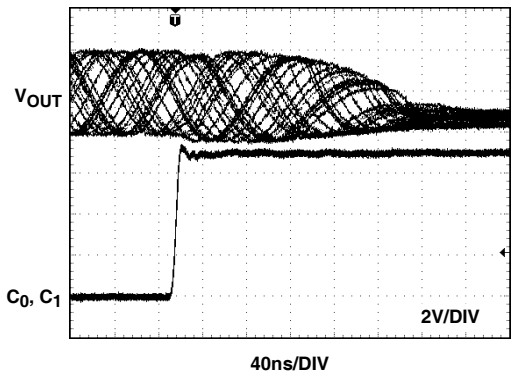


FIGURE 35. DISABLE TIME

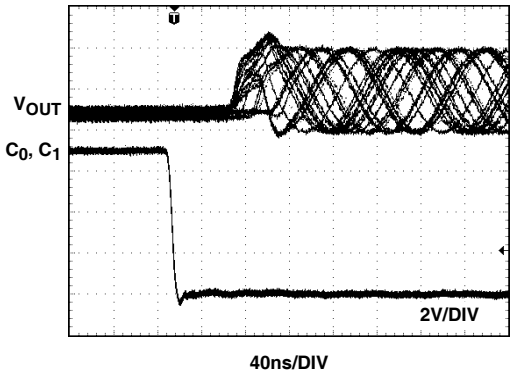


FIGURE 36. ENABLE TIME

Typical Performance Curves (Continued)

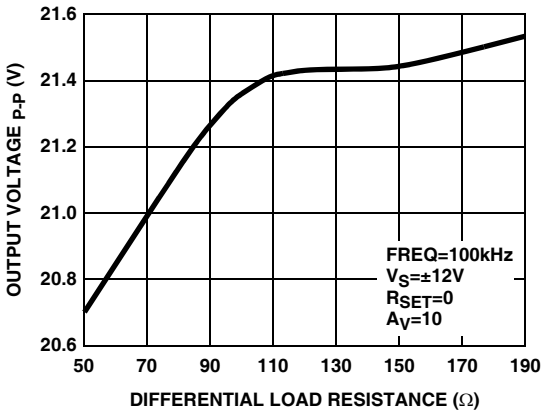


FIGURE 37. LOAD RESISTANCE vs OUTPUT VOLTAGE (ALL POWER MODES)

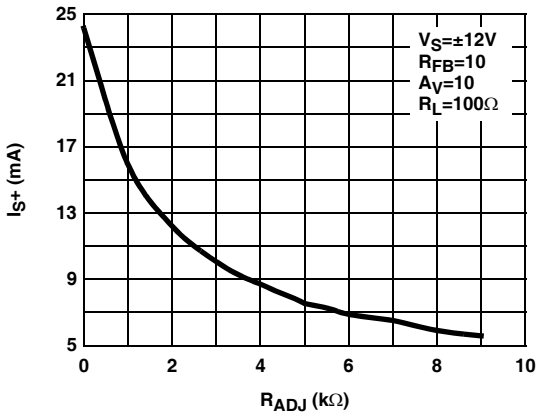


FIGURE 38. I_S+ vs R_{ADJ} (FULL POWER MODE)

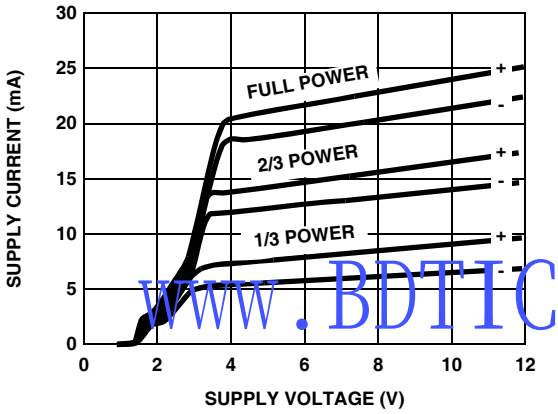


FIGURE 39. SUPPLY CURRENT vs SUPPLY VOLTAGE

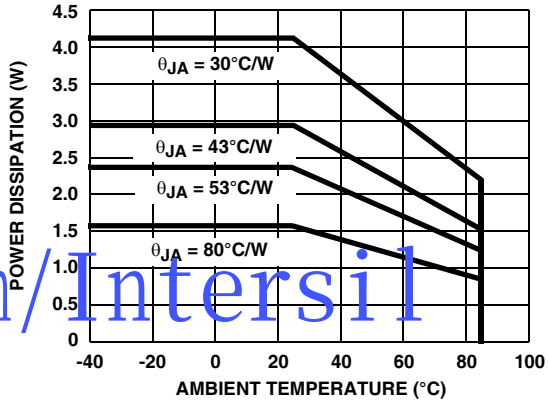


FIGURE 40. POWER DISSIPATION vs AMBIENT TEMPERATURE for VARIOUS MOUNTED θ_{JA}S (See Thermal Resistance Curve on page 15)

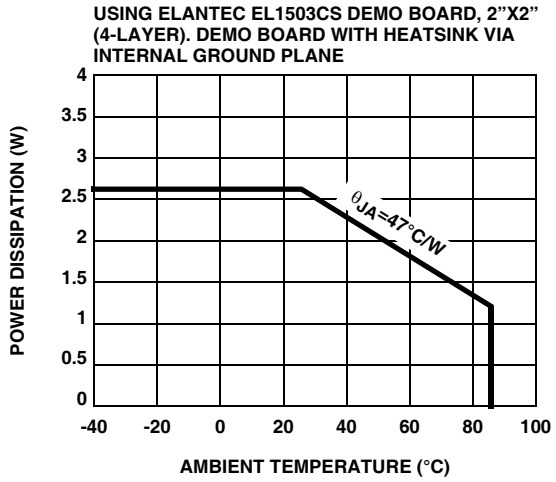


FIGURE 41. 16 LD SOIC POWER DISSIPATION and THERMAL RESISTANCE

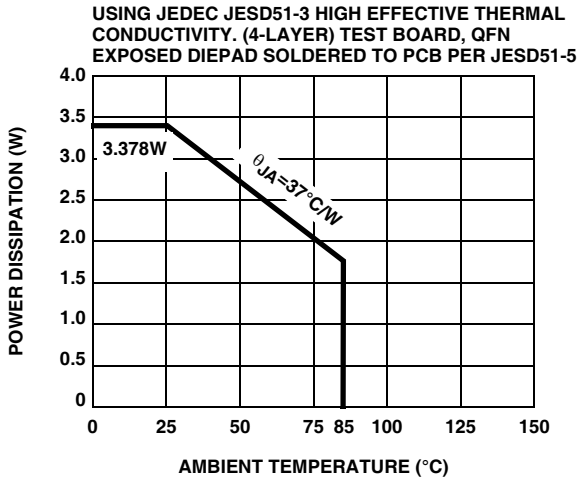


FIGURE 42. 24 LD QFN POWER DISSIPATION vs AMBIENT TEMPERATURE

Applications Information

The EL1508 consists of two high-power line driver amplifiers that can be connected for full duplex differential line transmission. The amplifiers are designed to be used with signals up to 4MHz and produce low distortion levels. The EL1508 has been optimized as a line driver for ADSL CO application. The driver output stage has been sized to provide full ADSL CO power level of 20dBM onto the telephone lines. Realizing that the actual peak output voltages and currents vary with the line transformer turns ratio, the EL1508 is designed to support 450mA of output current which exceeds the level required for 1:2 transformer ratio. A typical ADSL interface circuit is shown in Figure 43 below. Each amplifier has identical positive gain connections, and optimum common-mode rejection occurs. Further, DC input errors are duplicated and create common-mode rather than differential line errors.

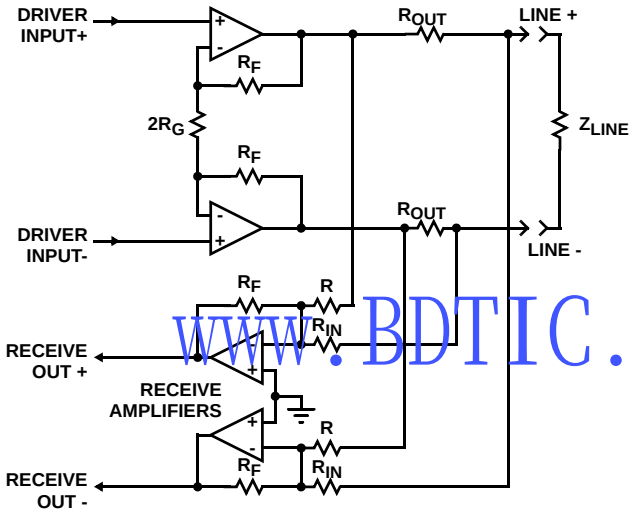


FIGURE 43. TYPICAL LINE INTERFACE CONNECTION

Input Connections

The EL1508 amplifiers are somewhat sensitive to source impedance. In particular, they do not like being driven by inductive sources. More than 100nH of source impedance can cause ringing or even oscillations. This inductance is equivalent to about 4” of unshielded wiring, or 6” of unterminated transmission line. Normal high-frequency construction obviates any such problem.

Power Supplies and Dissipation

Due to the high power drive capability of the EL1508, much attention needs to be paid to power dissipation. The power that needs to be dissipated in the EL1508 has two main contributors. The first is the quiescent current dissipation. The second is the dissipation of the output stage.

The quiescent power in the EL1508 is not constant with varying outputs. In reality, 50% of the total quiescent supply current needed to power each driver is converted in to output current. Therefore, in the equation below we should subtract the average output current, I_O, or 1/2 I_Q, whichever is the lowest. We’ll call this term I_X.

Therefore, we can determine a quiescent current with the equation:

$$P_{Dquiescent} = V_S \times (I_S - 21_X)$$

where:

V_S is the supply voltage (V_S+ to V_S-)

I_S is the operating supply current (I_S+ - I_S-) / 2

I_X is the lesser of I_O or 1/2 I_Q

The dissipation in the output stage has two main contributors. Firstly, we have the average voltage drop across the output transistor and secondly, the average output current. For minimal power dissipation, the user should select the supply voltage and the line transformer ratio accordingly. The supply voltage should be kept as low as possible, while the transformer ratio should be selected so that the peak voltage required from the EL1508 is close to the maximum available output swing. There is a trade off, however, with the selection of transformer ratio. As the ratio is increased, the receive signal available to the receivers is reduced.

Once the user has selected the transformer ratio, the dissipation in the output stages can be selected with the following equation:

$$P_{Dtransistors} = 2 \times \overline{I_O} \times \left(\frac{V_S}{2} - \overline{V_O}\right)$$

where:

V_S is the supply voltage (V_S+ to V_S-)

$\overline{V_O}$ is the average output voltage per channel

$\overline{I_O}$ is the average output current per channel

The overall power dissipation (P_{DISS}) is obtained by adding $P_{Dquiescent}$ and $P_{Dtransistor}$.

Estimating Line Driver Power Dissipation in ADSL CO Applications

Figure 44 on the following page shows a typical ADSL CO line driver implementation. The average line power requirement for the ADSL CO application is 20dBM (100mW) into a 100Ω line. The average line voltage is $3.16V_{RMS}$. The ADSL DMT peak to average ratio (crest factor) of 5.3 implies peak voltage of 16.7V into the line. Using a differential drive configuration and transformer coupling with standard back termination, a transformer ratio of 1:1 is selected. With 1:1 transformer ratio, the impedance across the driver side of the transformer is 100Ω, the average voltage is $3.16V_{RMA}$ and the average current is 31.6mA. The power dissipated in the EL1508 is a

combination of the quiescent power and the output stage power when driving the line:

$$Pd = P_{quiescent} + P_{output\text{-}stage}$$

$$Pd = V_S \times I_Q + (V_S - 2 \times V_{OUT\text{-}RMS}) \times I_{OUT\text{-}RMS}$$

In the full power mode and with 6.8k R_{ADJ} registers, the EL1508 consumes typically 7mA quiescent current and still able to maintain very low distortion. The distortion results are shown in typical performance section of the data sheet. When driving a load, a large portion (about 50%) of the quiescent current becomes output load current:

$$Pd = 12 \times (7mA \times 50\%) + (12V - 3.16) \times 31.6mA \times 2$$

where:

Pd = 598mW

The θ_{JA} requirement needs to be calculated. This is done using the equation:

$$\Theta_{JA} = \frac{T_{JUNCT} - T_{AMB}}{P_{DISS}}$$

where:

T_{JUNCT} is the maximum die temperature (150°C)

T_{AMB} is the maximum ambient temperature (85°C)

P_{DISS} is the dissipation calculated above

θ_{JA} is the junction to ambient thermal resistance for the package when mounted on the PCB

$$\Theta_{JA} = \frac{150 - 85}{598mW} = 108°C/W$$

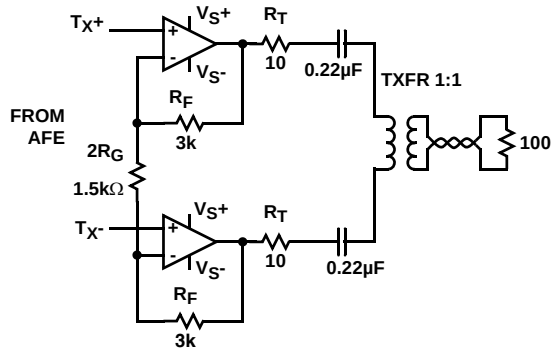
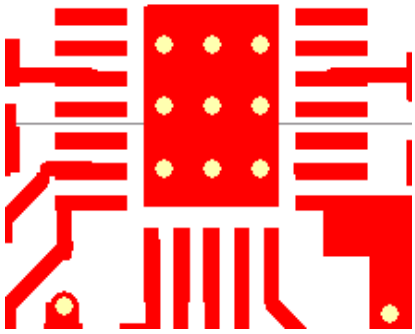


FIGURE 44. TYPICAL ADSL CO LINE DRIVER IMPLEMENTATION

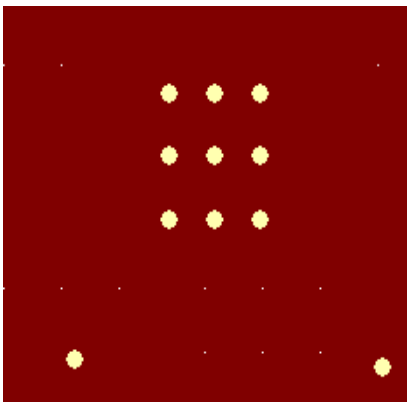
PCB Layout Considerations for QFN and SOIC Packages

The EL1508 die is packaged in three different thermally-efficient packages: a 20 Ld SOIC (0.300”), a 16 Ld SOIC (0.150”), and a 24 Ld QFN. The 16 Ld SOIC has the same external dimensions as a standard 0.150” width SOIC package, but has the center four leads (two per side) internally-fused for heat transfer purposes. Both packages can use PCB surface metal vias areas and internal ground planes, to spread heat away from the package. The larger the PCB area the lower the junction temperature of the device will be. In XDSL applications, multiple layer circuit boards with internal ground plane are generally used. 13 mil vias are recommended to connect the metal area under the device with the internal ground plane. Examples of the PCB layouts are shown in the figures below that result in thermal resistance θ_{JA} of 37°C/W for the QFN package and 47°C/W for the SOIC package. The thermal resistance is obtained with the EL1508CL and CS demo boards. The demo board is a 4-layer board built with 2oz. copper and has a dimension of $4in^2$. Note, the user must follow the thermal layout guideline to achieve these results. In addition to lower thermal resistance, the QFN package exhibits much lower 2nd harmonic distortion.

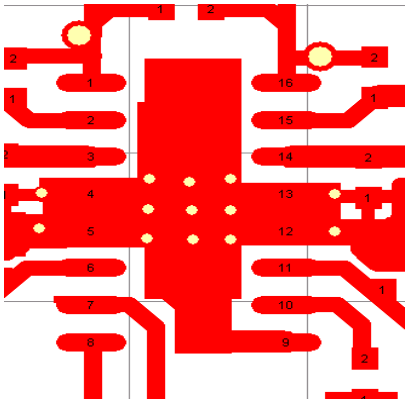
A separate Application Note for the QFN package and layout recommendations is also available.



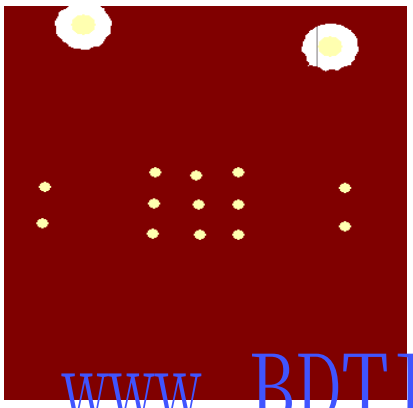
TOP (24 LD QFN)



INTERNAL GROUND PLANE (24 LD QFN)



TOP (16 Ld SO)



INTERNAL GROUND PLANE (16 Ld SO)

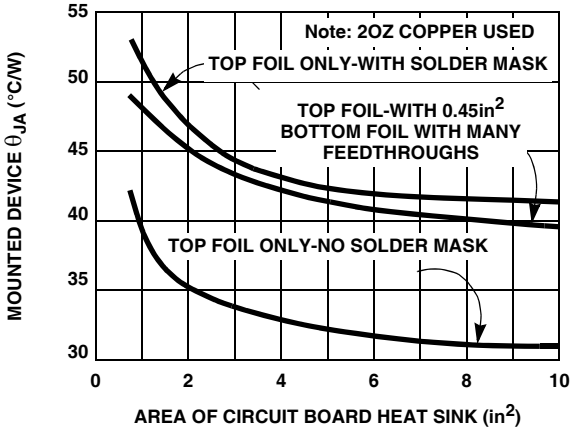


FIGURE 45. THERMAL RESISTANCE of 20 LD SO (0.300") EL1508 vs BOARD COPPER AREA

EL1508CM PCB Layout Considerations

The 20 Ld SOIC (0.300") Power Package is designed so that heat may be conducted away from the device in an efficient manner. To disperse this heat, the center four leads on either side of the package are internally fused to the mounting platform of the die. Heat flows through the leads into the circuit board copper, then spreads and convects to air. Thus, the ground plane on the component side of the board becomes the heatsink. This has proven to be a very effective technique, but several aspects of board layout should be noted. First, the heat should not be shunted to internal copper layers of the board nor backside foil, since the feedthroughs and fiberglass of the board are not very thermally conductive. To obtain the best thermal resistance of the mounted part, θ_{JA}, the topside copper ground plane should have as much area as possible and be as thick as practical. If possible, the solder mask should be cut away from the EL1508 to improve thermal resistance. Finally, metal heatsinks can be placed against the board close to the part to draw heat toward the chassis. The graph below shows various θ_{JA}s for the 20 Ld SOIC mounted on different copper foil areas.

Power Control Function

The EL1508 contains two forms of power control operation. Two digital inputs, C_0 and C_1, can be used to control the supply current of the EL1508 drive amplifiers. As the supply current is reduced, the EL1508 will start to exhibit slightly higher levels of distortion and the frequency response will be limited. The 4 power modes of the EL1508 are set up as shown in the following table:

TABLE 1. POWER MODES OF THE EL1508

C_1	C_0	OPERATION
0	0	I_S full power mode
0	1	2/3 I_S power mode
1	0	1/3 I_S power mode
1	1	Power-down

Another method for controlling the power consumption of the EL1508 is to connect a resistor from the I_{ADJ} pin to ground. When the I_{ADJ} pin is grounded (the normal state), the supply current per channel is as per the specifications table on page 2. When a resistor is inserted, the supply current is scaled according to the "R_{SET} vs I_S" graphs in the Performance Curves section.

Both methods of power control can be used simultaneously. In this case, positive and negative supply currents (per amp) are given by the equations below:

$$I_S+ = 0.9mA + \frac{12.4mA}{(1 + R_{SET} \div 1574\Omega)} \times (2/3\overline{C_1} + 1/3\overline{C_0})$$

$$I_S- = \frac{12.4mA}{(1 + R_{SET} \div 1574\Omega)} \times (2/3\overline{C_1} + 1/3\overline{C_0})$$

Output Loading

While the drive amplifiers can output in excess of 500mA transiently, the internal metallization is not designed to carry more than 100mA of steady DC current and there is no

current-limit mechanism. This allows safely driving rms sinusoidal currents of 2 x 100mA, or 200mA. This current is more than that required to drive line impedances to large output levels, but output short circuits cannot be tolerated. The series output resistor will usually limit currents to safe values in the event of line shorts. Driving lines with no series resistor is a serious hazard.

The amplifiers are sensitive to capacitive loading. More than 25pF will cause peaking of the frequency response. The same is true of badly terminated lines connected without a series matching resistor.

Output AC Coupling

When in power-down mode, several volts of differential voltage may appear across the line driver outputs. If DC current path exists between the two outputs, large DC current can flow from the positive supply rail to the negative supply rail through the outputs. To avoid DC current flow, the most effective solution is to place DC blocking capacitors in series at the outputs, as shown by the 0.22µF capacitors in Figure 44.

Power Supplies

The power supplies should be well bypassed close to the EL1508. A 2.2µF tantalum capacitor and a 0.1µF ceramic capacitor for each supply works well. Since the load currents are differential, they should not travel through the board copper and set up ground loops that can return to amplifier inputs. Due to the class AB output stage design, these currents have heavy harmonic content. If the ground terminal of the positive and negative bypass capacitors are connected to each other directly and then returned to circuit ground, no such ground loops will occur. This scheme is employed in the layout of the EL1508 demonstration board, and documentation can be obtained from the factory.

Single Supply Operation

The EL1508 can also be powered from a single supply voltage. When operating in this mode, the GND pins can still be connected directly to GND. To calculate power dissipation, the equations in the previous section should be used, with V_S equal to half the supply rail.

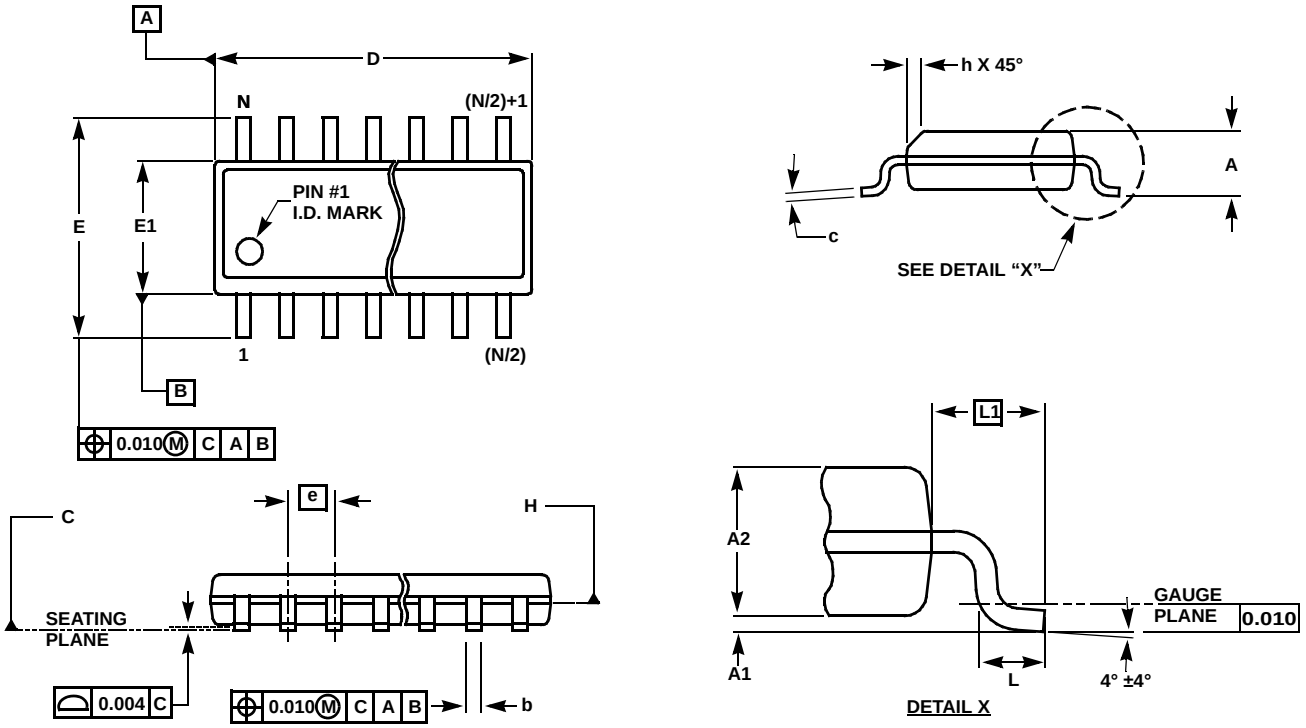
Feedback Resistor Value

The bandwidth and peaking of the amplifiers varies with supply voltage somewhat and with gain settings. The feedback resistor values can be adjusted to produce an optimal frequency response. Here is a series of resistor values that produce an optimal driver frequency response (1dB peaking) for different supply voltages and gains:

TABLE 2. OPTIMUM DRIVER FEEDBACK RESISTOR FOR VARIOUS GAINS AND SUPPLY VOLTAGES

SUPPLY VOLTAGE	DRIVER VOLTAGE GAIN		
	2.5	5	10
±5V	3.5k	3.25k	3k
±12V	3.5k	3.25k	3k

Small Outline Package Family (SO)



MDP0027

SMALL OUTLINE PACKAGE FAMILY (SO)

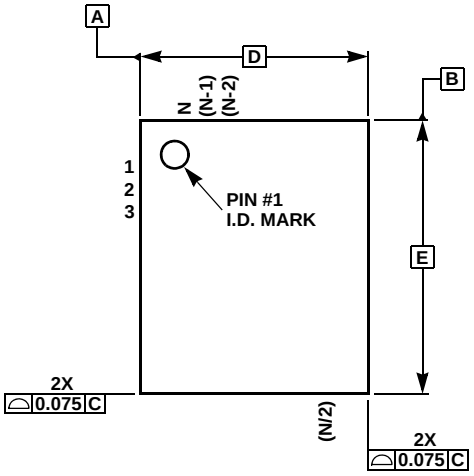
SYMBOL	INCHES							TOLERANCE	NOTES
	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)		
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX	-
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	±0.003	-
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	±0.002	-
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	±0.003	-
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	±0.001	-
D	0.193	0.341	0.390	0.406	0.504	0.606	0.704	±0.004	1, 3
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	±0.008	-
E1	0.154	0.154	0.154	0.295	0.295	0.295	0.295	±0.004	2, 3
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic	-
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	±0.009	-
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic	-
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference	-
N	8	14	16	16	20	24	28	Reference	-

Rev. M 2/07

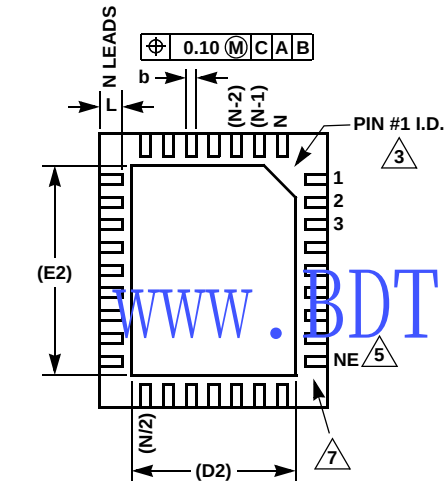
NOTES:

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994

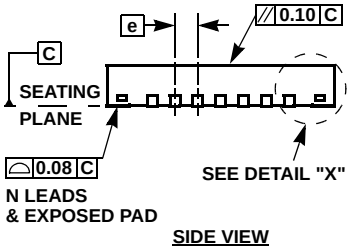
QFN (Quad Flat No-Lead) Package Family



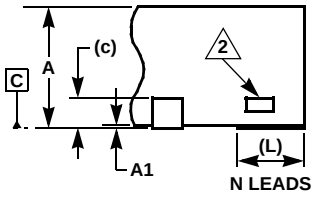
TOP VIEW



BOTTOM VIEW



SIDE VIEW



DETAIL X

MDP0046

QFN (QUAD FLAT NO-LEAD) PACKAGE FAMILY (COMPLIANT TO JEDEC MO-220)

SYMBOL	MILLIMETERS				TOLERANCE	NOTES
	QFN44	QFN3	QFN32			
A	0.90	0.90	0.90	0.90	±0.10	-
A1	0.02	0.02	0.02	0.02	+0.03/-0.02	-
b	0.25	0.25	0.23	0.22	±0.02	-
c	0.20	0.20	0.20	0.20	Reference	-
D	7.00	5.00	8.00	5.00	Basic	-
D2	5.10	3.80	5.80	3.60/2.48	Reference	8
E	7.00	7.00	8.00	6.00	Basic	-
E2	5.10	5.80	5.80	4.60/3.40	Reference	8
e	0.50	0.50	0.80	0.50	Basic	-
L	0.55	0.40	0.53	0.50	±0.05	-
N	44	38	32	32	Reference	4
ND	11	7	8	7	Reference	6
NE	11	12	8	9	Reference	5

SYMBOL	MILLIMETERS					TOLER-ANCE	NOTES
	QFN28	QFN2	QFN20		QFN16		
A	0.90	0.90	0.90	0.90	0.90	±0.10	-
A1	0.02	0.02	0.02	0.02	0.02	+0.03/ -0.02	-
b	0.25	0.25	0.30	0.25	0.33	±0.02	-
c	0.20	0.20	0.20	0.20	0.20	Reference	-
D	4.00	4.00	5.00	4.00	4.00	Basic	-
D2	2.65	2.80	3.70	2.70	2.40	Reference	-
E	5.00	5.00	5.00	4.00	4.00	Basic	-
E2	3.65	3.80	3.70	2.70	2.40	Reference	-
e	0.50	0.50	0.65	0.50	0.65	Basic	-
L	0.40	0.40	0.40	0.40	0.60	±0.05	-
N	28	24	20	20	16	Reference	4
ND	6	5	5	5	4	Reference	6
NE	8	7	5	5	4	Reference	5

Rev 11 2/07

NOTES:

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Tiebar view shown is a non-functional feature.
3. Bottom-side pin #1 I.D. is a diepad chamfer as shown.
4. N is the total number of terminals on the device.
5. NE is the number of terminals on the “E” side of the package (or Y-direction).
6. ND is the number of terminals on the “D” side of the package (or X-direction). ND = (N/2)-NE.
7. Inward end of terminal may be square or circular in shape with radius (b/2) as shown.
8. If two values are listed, multiple exposed pad options are available. Refer to device-specific datasheet.