Fairchild Semiconductor Application Note March 1999 Revised December 2000



PC100 Memory Driver Competitive Comparisons

Introduction

Overview

The latest developments in chipset and motherboard design have taken memory performance requirements to new levels. The memory bus speed has been increased from 66MHz to 100MHz to keep pace with the needs of advanced operating systems and software. Feeding today's PC/workstation/server often requires large banks of dense SDRAM (Synchronous DRAM) ICs arranged on DIMMs (Dual in-line memory modules). Due to the inability of the system memory controller to drive the large amount of memory devices and maintain signal integrity or system timing requirements, many of today's DIMMs require buffering of the address and control signal paths. Intel has published a specification for 100MHz SDRAM memory modules called PC100. Proper selection of the logic devices to register and redrive heavily loaded address and control signal paths requires careful consideration of device parameters and can result in a SDRAM DIMM design that uses the fewest components and provides reliable circuit performance (Note 1). This application note compares Fairchild Semiconductor's logic solutions for buffered (or registered) DIMMs to other competitive solutions.

Note 1: See Fairchild Semiconductor AN-5003 PC100 SDRAM Memory Driver Solutions

Fairchild Semiconductor's *CROSSVOLT*[™] VCX family offers a variety of logic solutions that meet or exceed the PC100 specification.

Device#	Function
74VCX16835	18 Bit Universal Buffer
74VCX162835	18 Bit Universal Buffer w/ 25 Ω Resistor
74VCX16838	16 Bit Selectable Register Buffer
74VCX162838	16 Bit Selectable Register Buffer w/ 25 Ω Resistor
74VCX16839	20 Bit Selectable Register Buffer
74VCX162839	20 Bit Selectable Register Buffer

The information in this application note provides functional and specification comparisons to several ALVC devices that are also used in DIMM applications. There are several device number differences between the two families. The table below provides a cross reference between VCX and ALVC. AN-5005 PC100 Memory Driver Competitive Comparisons

Fairchild Device#	ALVC Device #	Function								
74VCX16835	74ALVC16835	18 Bit Universal Buffer								
74VCX162835	74ALVC162835	18 Bit Universal Buffer w/ 25 Ω Resistor								
74VCX16838	74ALVC16334	16 Bit Selectable Register Buffer								
74VCX162838	74ALVC162334	16 Bit Selectable Register Buffer w/ 25 Ω Resistor								
74VCX16839	74ALVC16836	20 Bit Selectable Register Buffer								
74VCX162839	74ALVC162836	20 Bit Selectable Register Buffer w/ 25 Ω Resistor								

VCX and ALVC Cross Reference Table

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Comparison of 74VCX16835 vs. 74ALVC16835

Part Descriptions

Connection Diagram

NC

NC 2 56 - GND

55 **NC**

74VCX16835	18 Bit Universal Buffer with 3-STATE Outputs
74ALVC16835	18 Bit Universal Buffer
	with 3-STATE Outputs

Functional Comparison

The 74VCX16835 and 74ALVC16835 are pin and functionally equivalent.

Function Table

	Inputs									
OE	LE	CLK	I _n	On						
Н	Х	х	Х	Z						
L	н	х	L	L						
L	н	х	н	н						
L	L	\uparrow	L	L						
L	L	Ŷ	н	н						
L	L	н	Х	I ₀ (Note 2)						
L	L	L	Х	I ₀ (Note 3)						

 $\begin{array}{l} H = \mbox{Logic HIGH} \\ \mbox{L} = \mbox{Logic LOW} \\ X = \mbox{Don't Care, but not floating} \\ \mbox{Z} = \mbox{High Impedance} \\ \mbox{\uparrow} = \mbox{LOW-to-HIGH Transition} \end{array}$

Note 2: Output level before the indicated steady-state input conditions were established provided that CLK was HIGH before LE went LOW. Note 3: Output level before the indicated steady-state input conditions were established.

0 ₁	3	54	I1
GND	4	53	-GND
0 ₂ _	5	52	-1 ₂
о _з _	6	51	I ₃
Vcc -	7	50	-v _{cc}
а ₄ —	8	49	— I ₄
0 ₅ —	9	48	— I ₅
0 ₆ —	10	47	 I ₆
GND -	11	46	- GND
0 ₇ -	12	45	- 1 ₇
0 ₈ —	13	44	— I ₈
0 ₉ _	14	43	_l9
0 ₁₀ —	15	42	I ₁₀
011 -	16	41	I ₁₁
0 ₁₂ –	17	40	-1 ₁₂
GND 🗕	18	39	- GND
0 ₁₃ –	19	38	I ₁₃
0 ₁₄	20	37	I ₁₄
0 ₁₅ -	21	36	- I ₁₅
V _{CC} -	22	35	- Vcc
0 ₁₆ —	23	34	
0 ₁₇ —	24	33	
GND -	25	32	- GND
0 ₁₈ —	26	31	I ₁₈
OE -	27	30	-CLK
LE -	28	29	- GND



Comparison of 74VCX16835 vs. 74ALVC16835 (Continued) AC Comparison

The following table shows a comparison of the 74VCX16835 device and the equivalent ALVC device. The table also compares performance vs. the Intel PC100 Rev 1.2 Registered DIMM specification.

AC Specifications Table

Baramatar	Symbol	PC100 (1.2)		74VCX16835		74ALVC16835		11:40	Tool Conditions
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Units	Test Conditions
CLK Input Capacitance	C _{IN}	3.30	6.00	3.5	(Тур)	3.5	(Тур)	pF	10 MHz
Maximum Clock Frequency	f _{MAX}	150		250		150		MHz	
Output Edge Rate	t _{THL/LH}	1.00	2.50					V/ns	C _L = 50pF V _{CC} = 3.3V +/- 0.15V Between 1.2V -1.8V
Propagation Delay – Register	t _{PHL/LH} CLK to Y	1.7	4.5	1.7	4.5	1.7	4.5	ns	C _L = 50pF V _{CC} = 3.3V +/- 0.15V CLK to any Y
Propagation Delay – Register	t _{PHL/LH} CLK to Y	1.5	3.0	1.5	3.0	1.5	2.9	ns	C _L = 0pF V _{CC} = 3.3V +/- 0.15V CLK to any Y
Propagation Delay – Buffer	t _{PHL/LH} A to Y	1.0	4.5	1.0	3.6	1.0	4.0	ns	C _L = 50pF V _{CC} = 3.3V +/- 0.15V A to any Y
Propagation Delay – Buffer	t _{PHL/LH} A to Y	0.9	2.0	0.7	2.1	0.9	2.0	ns	C _L = 0pF V _{CC} = 3.3V +/- 0.15V A to any Y
Maximum Allowable SSO Delay			300					ps	C_L = 50pF, Any output combination, V_{CC} = 3.3V +/- 0.15V
Setup Time	t _{SET}	1.7		1.5		1.7		ns	V _{CC} = 3.3V +/- 0.15V Any input
Hold Time	t _{HOLD}	0.7		0.7		0.7		ns	V _{CC} = 3.3V +/- 0.15V Any input
Input Current	I _{IN}		10.0		5.0		5.0	uA	V _{IN} = 0V to 3.45V V _{CC} = 3.3V +/- 0.15V

Note: AC Specifications Table for the VCX and ALVC products above are for V_{CC} = \pm 10%, and T_A = –40 to 85°C

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Comparison of 74VCX162835 vs. 74ALVC162835

Part Descriptions		Co	Connection Diagram				
74VCX162835	18 Bit Universal Buffer with 3-STATE Outputs and 25 Ω Resistors	NC	1 5 2 5	6 GND 5 NC			
74ALVC162835	18 Bit Universal Buffer with 3-STATE Outputs and 25 O Recistors	0 ₁ — GND —	3 5 4 5	4 — I₁ 3 — GND			
		0 ₂ _	5 5	2 -12			
Functional Compa	rison	0 ₃ —	6 5	1 — I ₃			
The 74VCX162835	and 74ALVC162835 are pin and func-	Vcc —	7 5	0 – Vcc			

The 74VCX162835 and 74ALVC162835 are pin and functionally equivalent.

Function Table

	Inputs									
OE	LE	CLK	I _n	0 _n						
н	Х	х	Х	Z						
L	н	х	L	L						
L	н	х	н	н						
L	L	\uparrow	L	L						
L	L	Ŷ	н	н						
L	L	н	Х	I _o (Note 4)						
L	L	L	Х	I _o (Note 5)						

H = Logic HIGHL = Logic LOW X = Don't Care, but not floating

Z = High Impedance $\uparrow = LOW-to-HIGH Transition$

Note 4: Output level before the indicated steady-state input conditions were established provided that CLK was HIGH before LE went LOW.

Note 5: Output level before the indicated steady-state input conditions were established.

0 ₇ -	12	45	- 1 ₇
0 ₈ —	13	44	I ₈
0 ₉ _	14	43	— ¹ 9
0 ₁₀ —	15	42	-1 ₁₀
0 ₁₁ —	16	41	I ₁₁
0 ₁₂ —	17	40	-1 ₁₂
GND -	18	39	- GND
0 ₁₃ –	19	38	- I ₁₃
0 ₁₄ _	20	37	-1 ₁₄
0 ₁₅ -	21	36	- I ₁₅
V _{CC}	22	35	- Vcc
0 ₁₆ —	23	34	-1 ₁₆
0 ₁₇ -	24	33	- 1 ₁₇
GND -	25	32	- GND
0 ₁₈ -	26	31	-1 ₁₈
OE -	27	30	-CLK
LE	28	29	- GND

49

48 **-** I₅

47 • I₆

46 -GND

- I4

a₄

05

06 10

GND 11

8

9



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4

Comparison of 74VCX162835 vs. 74ALVC162835 (Continued) AC Comparison

The following table shows a comparison of the 74VCX162835 device and the equivalent ALVC device. The table also compares performance vs. the Intel PC100 Rev 1.2 Registered DIMM specification.

AC Specifications Table

Paramotor	Symbol	PC100 (1.2) 74VCX162835		(162835	74ALVC162835		Unite	Toot Conditions	
Farameter	Symbol	Min	Max	Min	Max	Min	Max	Units	Test conditions
CLK Input Capacitance	C _{IN}	3.30	6.00	3.5	(Тур)	3.5	(Тур)	pF	10 MHz
Maximum Clock Frequency	f _{MAX}	150		250		150		MHz	
Output Edge Rate	t _{THL/LH}	1.00	2.50					V/ns	C _L = 50pF V _{CC} = 3.3V +/- 0.15V Between 1.2V -1.8V
Propagation Delay – Register	t _{PHL/LH} CLK to Y	1.9	4.5	1.9	4.5	1.9	5.0	ns	C _L = 50pF V _{CC} = 3.3V +/- 0.15V CLK to any Y
Propagation Delay – Register	t _{PHL/LH} CLK to Y	1.4	2.9	1.4	2.9	1.4	2.9	ns	C _L = 0pF V _{CC} = 3.3V +/- 0.15V CLK to any Y
Propagation Delay – Buffer	t _{PHL/LH} A to Y	1.0	4.5	1.0	4.2	1.0	4.0	ns	C _L = 50pF V _{CC} = 3.3V +/- 0.15V A to any Y
Propagation Delay – Buffer	t _{PHL/LH} A to Y	0.9	2.0	0.7	2.6	0.9	2.0	ns	C _L = 0pF V _{CC} = 3.3V +/- 0.15V A to any Y
Maximum Allowable SSO Delay			300					ps	C_L = 50pF, Any output combination, V_{CC} = 3.3V +/- 0.15V
Setup Time	t _{SET}	1.7		1.5		1.7		ns	V _{CC} = 3.3V +/- 0.15V Any input
Hold Time	t _{HOLD}	0.7		0.7		0.7		ns	V _{CC} = 3.3V +/- 0.15V Any input
Input Current	I _{IN}	1.9	4.5	1.9	4.5	1.9	5.0	uA	V _{IN} = 0V to 3.45V V _{CC} = 3.3V +/- 0.15V

Note: AC Specifications Table for the VCX and ALVC products above are for V_{CC} = \pm 10%, and T_A = –40 to 85°C

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Comparison of 74VCX16838 vs. 74ALVC16334

Part Descriptions	
74VCX16838	16 Bit Selectable Register Buffer with 3-STATE Outputs
74ALVC16334	16 Bit Universal Bus Driver with 3-STATE Outputs

Functional Comparison

The 74VCX16838 and 74ALVC16334 are pin and functionally equivalent for registered DIMM applications.

This means that one will see no functional difference when used in a registered DIMM application. There is however differences in the actual function of the devices. The 74VCX16838 was designed specifically for the Intel PC100 Rev 1.2 Registered DIMM specification and supports two modes of operation: a registered mode and a flow through mode. The 74ALVC16334 has additional functionality not required by the Intel PC100 Rev 1.2 Registered DIMM specification. While these devices support registered mode and flow through mode they have an additional latch mode.

Function Table for 74VCX16838

	Inputs									
CLK	REGE	0 _n								
\uparrow	Н	Н	L	н						
↑	н	L	L	L						
х	L	н	L	н						
х	L	L	L	L						
х	Х	х	н	Z						

Connection Diagram for 74VCX16838								
		48	- CLK					
0. –	2	47	— la					
-0 0. —	3	4.6	-0 					
	4	4.5	GND					
0	5	44	— Ia					
0 ₂	6	43						
v	7	42						
'cc	8	41	*cc					
°4	0	40	'4					
05	5	40	- '5 - CND					
	10	29	GND					
0 ₆ —	11	38	- ¹ 6					
0 ₇ —	12	37	- I ₇					
0 ₈ —	13	36	— I ₈					
0 ₉ —	14	35	— I ₉					
GND —	15	34	- GND					
0 ₁₀ —	16	33	— I ₁₀					
0 ₁₁ —	17	32	— I ₁₁					
v _{cc} –	18	31	– v _{cc}					
0 ₁₂ —	19	30	— I ₁₂					
0 ₁₃ —	20	29	— I _{1 3}					
gnd —	21	28	— GND					
0 ₁₄ —	22	27	— I _{1 4}					
0 ₁₅ —	23	26	— I ₁₅					
NC —	24	25	REGE					

H = Logic HIGH

L = Logic LOW

X = Don't Care, but not floating

Z = High Impedance $\uparrow =$ LOW-to-HIGH Transition





7



Comparison of 74VCX16838 vs. 74ALVC16334 (Continued)

When the devices are in registered or flow through mode they will behave as functional equivalents. The waveforms shown in Figure 1 show how the devices respond in flow through and registered modes.



FIGURE 1. Flow Through Mode Waveforms

The actual functional differences can only be seen by transitioning the $REGE(\overline{LE})$ pin when the data latched into the internal register is different from the data on the input port. The waveforms to generate this condition are shown in Figure 2. The 74VCX16838 is implemented such that the REGE pin selects between the flow through mode and the registered modes. The 74ALVC16334 is implemented such that the LE pin will force the internal latches enabled and pass data through these latches in flow-through mode.



FIGURE 2. Transitioning Waveforms

The functional differences shown do not impact registered DIMM Module application because the REGE pin is typically fixed in one state or the other for a given application. The implementation chosen for the 74VCX16838 was done to provide improved AC performance in flow-through mode.

Comparison of 74VCX16838 vs. 74ALVC16334 (Continued) AC Comparison

The following table shows a comparison of the 74VCX16838 device and the equivalent ALVC device. The table also compares performance vs. the Intel PC100 Rev 1.2 Registered DIMM specification.

AC Specifications Table

Paramotor	Symbol	PC10	0 (1.2)	74VC)	K16838	74ALV	C16334	Unite	Tost Conditions
Farameter	Symbol	Min	Max	Min	Max	Min	Max	Units	Test conditions
CLK Input Capacitance	C _{IN}	3.30	6.00	3.5	(Тур)	3.5	(Тур)	pF	10 MHz
Maximum Clock Frequency	f _{MAX}	150		250		150		MHz	
Output Edge Rate	t _{THL/LH}	1.00	2.50					V/ns	C _L = 50pF V _{CC} = 3.3V +/- 0.15V Between 1.2V -1.8V
Propagation Delay – Register	t _{PHL/LH} CLK to Y	1.7	4.5	1.1	3.3	1.0	4.1	ns	C _L = 50pF V _{CC} = 3.3V +/- 0.15V CLK to any Y
Propagation Delay – Register	t _{PHL/LH} CLK to Y	1.5	3.0					ns	C _L = 0pF V _{CC} = 3.3V +/- 0.15V CLK to any Y
Propagation Delay – Buffer	t _{PHL/LH} A to Y	1.0	4.5	1.1	2.8	1.1	3.3	ns	C _L = 50pF V _{CC} = 3.3V +/- 0.15V A to any Y
Propagation Delay – Buffer	t _{PHL/LH} A to Y	0.9	2.0					ns	C _L = 0pF V _{CC} = 3.3V +/- 0.15V A to any Y
Maximum Allowable SSO Delay			300					ps	C_L = 50pF, Any output combination, V_{CC} = 3.3V +/- 0.15V
Setup Time	t _{SET}	1.7		1.5		1.5		ns	V _{CC} = 3.3V +/- 0.15V Any input
Hold Time	t _{HOLD}	0.7		1.0		0.9		ns	V _{CC} = 3.3V +/- 0.15V Any input
Input Current	I _{IN}		10.0		5.0		5.0	uA	V _{IN} = 0V to 3.45V V _{CC} = 3.3V +/- 0.15V

Note: AC Specifications Table for the VCX and ALVC products above are for V_{CC} = \pm 10%, and T_A = –40 to 85°C

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Comparison of 74VCX162838 vs. 74ALVC162334

Part Descriptions

74VCX162838 16 Bit Selectable Register Buffer with 3-STATE Outputs and 25Ω Resistors

74ALVC162334 16 Bit Universal Bus Driver with 3-STATE

Outputs and 25Ω Resistors

Functional Comparison

The 74VCX162838 and 74ALVC162334 are pin and functionally equivalent for registered DIMM applications.

This means that one will see no functional difference when used in a registered DIMM application. There is however differences in the actual function of the devices. The 74VCX162838 was designed specifically for the Intel PC100 Rev 1.2 Registered DIMM specification and supports two modes of operation: a registered mode and a flow through mode. The 74ALVC162334 has additional functionality not required by the Intel PC100 Rev 1.2 Registered DIMM specification. While these devices support registered mode and flow through mode and flow through mode they have an additional latch mode.

When the devices are in registered or flow through mode they will behave as functional equivalents. The waveforms shown in Figure 1 show how the devices respond in flow through and registered modes.

The actual functional differences can only be seen by transitioning the REGE($\overline{\text{LE}}$) pin when the data latched into the internal register is different from the data on the input port. The waveforms to generate this condition are shown in Figure 2. The 74VCX162838 is implemented such that the REGE pin selects between the flow through mode and the registered modes. The 74ALVC162334 is implemented such that the $\overline{\text{LE}}$ pin will force the internal latches enabled and pass data through these latches in flow-through mode. The functional differences shown do not impact registered DIMM Module application because the REGE pin is typically fixed in one state or the other for a given application. The implementation chosen for the 74VCX162838 was done to provide improved AC performance in flow-through mode.

Function Table for 74VCX162838

	Outputs			
CLK	REGE	I _n	OE	On
↑	Н	Н	L	Н
\uparrow	н	L	L	L
Х	L	н	L	н
Х	L	L	L	L
Х	Х	х	н	Z

H = Logic HIGH

L = Logic LOW

X = Don't Care, but not floating

Z = High Impedance ↑ = LOW-to-HIGH Transition

Connection Diagram for 74VCX162838

ŌE —	1	\bigcirc	48	- CLK
0 ₀ —	2		47	— I ₀
0 ₁ —	3		46	— i
GND —	4		45	— GND
0 ₂ —	5		44	- I ₂
0 ₃ —	6		43	- I ₃
v _{cc} –	7		42	-v _{cc}
04 -	8		41	- I4
0 ₅ —	9		40	— I ₅
GND —	10		39	— GND
0 ₆ —	11		38	— I ₆
0 ₇ —	12		37	-1 ₇
°8 —	13		36	— I ₈
0 ₉ —	14		35	— I ₉
GND —	15		34	— GND
0 ₁₀ —	16		33	- I ₁₀
0 ₁₁ —	17		32	-41
v _{cc} –	18		31	-v _{cc}
0 ₁₂	19		30	- I ₁₂
0 ₁₃ —	20		29	- ' ₁₃
GND —	21		28	— GND
0 ₁₄ —	22		27	- I ₁₄
0 ₁₅ —	23		26	- 4 ₁₅
NC -	24		25	- REGE

Logic Diagram for 74VCX162838





Comparison of 74VCX162838 vs. 74ALVC162334 (Continued) AC Comparison

The following table shows a comparison of the 74VCX162838 device and the equivalent ALVC device. The table also compares performance vs. the Intel PC100 Rev 1.2 Registered DIMM specification.

AC Specifications Table

Peromotor	Symbol	PC10	0 (1.2)	74VCX	162838	74ALV	C162334	Unito	Toot Conditions
Farameter	Symbol	Min	Max	Min	Max	Min	Max	Units	Test Conditions
CLK Input Capacitance	C _{IN}	3.30	6.00	6.0	(Тур)	5.0	(Тур)	pF	10 MHz
Maximum Clock Frequency	f _{MAX}	150		200		150		MHz	
Output Edge Rate	t _{THL/LH}	1.00	2.50					V/ns	C _L = 50pF V _{CC} = 3.3V +/- 0.15V Between 1.2V -1.8V
Propagation Delay – Register	t _{PHL/LH} CLK to Y	1.9	4.5	1.1	4.2	1.0	4.9	ns	C _L = 50pF V _{CC} = 3.3V +/- 0.15V CLK to any Y
Propagation Delay – Register	t _{PHL/LH} CLK to Y	1.4	2.9					ns	C _L = 0pF V _{CC} = 3.3V +/- 0.15V CLK to any Y
Propagation Delay – Buffer	t _{PHL/LH} A to Y	1.0	4.5	1.1	3.8	1.1	3.9	ns	C _L = 50pF V _{CC} = 3.3V +/- 0.15V A to any Y
Propagation Delay – Buffer	t _{PHL/LH} A to Y	0.9	2.0					ns	C _L = 0pF V _{CC} = 3.3V +/- 0.15V A to any Y
Maximum Allowable SSO Delay			300					ps	C_L = 50pF, Any output combination, V_{CC} = 3.3V +/- 0.15V
Setup Time	t _{SET}	1.7		1.5		1.5		ns	V _{CC} = 3.3V +/- 0.15V Any input
Hold Time	t _{HOLD}	0.7		1.0		0.9		ns	V _{CC} = 3.3V +/- 0.15V Any input
Input Current	I _{IN}		10.0		5.0		5.0	uA	V _{IN} = 0V to 3.45V V _{CC} = 3.3V +/- 0.15V

Note: AC Specifications Table for the VCX and ALVC products above are for V_{CC} = \pm 10%, and T_A = –40 to 85°C

•		27.10000		Connectio	n Diagram for	74VC¥1693
art Descriptio	ns			Connectio		
4VCX16839	20 Bit Seleo with 3-STA	ctable Register TE Outputs	Buffer	OE -		56 — CLK
4ALVC16836	20 Bit Unive	ersal Bus Drive	r	°° —	2	55 — I ₀
	with 3-STA	I E Outputs		0 ₁ —	3	54 — I ₁
ctional Comp	arison			GND —	4	53 — GND
74VCX16839	and 74ALVC	16836 are pin a	nd function-	0 ₂ —	5	52 – I ₂
equivalent for r	egistered DI	MM applications	6.	0 ₃ —	6	51 — I ₃
				v _{cc} —	7	50 — V _{CC}
means that or	ne will see no	functional diffe	rence when	0 ₄ —	8	49 I ₄
d in a registere	ed DIMM app	blication. There	is however	0 ₅ —	9	48 — I ₅
CX16839 was	designed sne	cifically for the	Intel PC100	0 ₆ —	10	47 - I ₆
1.2 Registere	d DIMM spec	cification and s	upports two	GND —	11	46 — GND
les of operation	n: a registere	d mode and a f	low through	0 ₇ —	12	45 🗖 I ₇
le. The 74ALV	C16836 has	additional func	tionality not	0 ₈ —	13	44 - I ₈
urea by the Ir	these device	sev 1.2 Regist	ered DIMM	0 ₉ —	14	43 🗖 Ig
flow through m	ode they hav	e an additional	latch mode.	0 ₁₀ —	15	42 - I ₁₀
Funct	ion Table for	74VCX16839		0 ₁₁ —	16	4 1 🗕 I _{1 1}
		. ++ 0/10039	1 1	0 ₁₂ —	17	40 - I ₁₂
	Inputs		Outputs	GND -	18	39 — GND
CLK RE	GE I _n	OE	On	0 ₁₃ —	19	38 — I ₁₃
↑ ∟		1		0 ₁₄ —	20	37 — I ₁₄
т П 	, п	L		0 ₁₅ —	21	36 — I ₁₅
r H	i L	L		v _{cc} —	22	35 — V _{CC}
X L	. н	L	н	0 ₁₆ —	23	34 - 1 ₁₆
X L	. L	L	L	0 ₁₇ —	24	33 - I ₁₇
x x	x	н	7	GND —	25	32 GND
	. ^		-	0,8 -	26	31 - I ₁₈
Logic LOW				0 ₁₉ —	27	30 - 49
Jon't Care, but not	floating			NC —	28	29 REGE
.OW-to-HIGH Trans	sition					
		Lo	gic Diagram fo	or 74VCX16839		
			To	19 Other Channels		
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Comparison of 74VCX16839 vs. 74ALVC16836 (Continued)



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FIGURE 3. Flow Through Mode Waveforms

The actual functional differences can only be seen by transitioning the $\text{REGE}(\overline{\text{LE}})$ pin when the data latched into the internal register is different from the data on the input port. The waveforms to generate this condition are shown in Figure 4. The 74VCX16839 is implemented such that the REGE pin selects between the flow through mode and the registered modes. The 74ALVC16836 is implemented such that the $\overline{\text{LE}}$ pin will force the internal latches enabled and pass data through these latches in flow-through mode.



FIGURE 4. Flow Through Mode Waveforms

The functional differences shown do not impact registered DIMM Module application because the REGE pin is typically fixed in one state or the other for a given application. The implementation chosen for the 74VCX16839 was done to provide improved AC performance in flow-through mode.

Comparison of 74VCX16839 vs. 74ALVC16836 (Continued) AC Comparison

The following table shows a comparison of the 74VCX16839 device and the equivalent ALVC device. The table also compares performance vs. the Intel PC100 Rev 1.2 Registered DIMM specification.

AC Specifications Table

Peromotor	Symbol	PC10	0 (1.2)	74VC)	(16839	74ALV	C16836	Unito	Toot Conditions
Farameter	Symbol	Min	Max	Min	Max	Min	Max	Units	Test Conditions
CLK Input Capacitance	C _{IN}	3.30	6.00	6.0	(Тур)	5.0	(Тур)	pF	10 MHz
Maximum Clock Frequency	f _{MAX}	150		250		150		MHz	
Output Edge Rate	t _{THL/LH}	1.00	2.50					V/ns	C _L = 50pF V _{CC} = 3.3V +/- 0.15V Between 1.2V -1.8V
Propagation Delay – Register	t _{PHL/LH} CLK to Y	1.7	4.5	1.1	3.8	1.4	4.5	ns	C _L = 50pF V _{CC} = 3.3V +/- 0.15V CLK to any Y
Propagation Delay – Register	t _{PHL/LH} CLK to Y	1.5	3.0					ns	C _L = 0pF V _{CC} = 3.3V +/- 0.15V CLK to any Y
Propagation Delay – Buffer	t _{PHL/LH} A to Y	1.0	4.5	1.1	2.8	1.0	3.6	ns	C _L = 50pF V _{CC} = 3.3V +/- 0.15V A to any Y
Propagation Delay – Buffer	t _{PHL/LH} A to Y	0.9	2.0					ns	C _L = 0pF V _{CC} = 3.3V +/- 0.15V A to any Y
Maximum Allowable SSO Delay			300					ps	C_L = 50pF, Any output combination, V_{CC} = 3.3V +/- 0.15V
Setup Time	t _{SET}	1.7		1.5		1.5		ns	V _{CC} = 3.3V +/- 0.15V Any input
Hold Time	t _{HOLD}	0.7		1.0		0.9		ns	V _{CC} = 3.3V +/- 0.15V Any input
Input Current	I _{IN}		10.0		5.0		5.0	uA	V _{IN} = 0V to 3.45V V _{CC} = 3.3V +/- 0.15V

Note: AC Specifications Table for the VCX and ALVC products above are for V_{CC} = \pm 10%, and T_A = –40 to 85°C

Comparison of 74VCX162839 vs. 74ALVC162836

Part Descriptions

 74VCX162839
 20 Bit Selectable Register Buffer with 3-STATE Outputs and 25Ω Resistors

 74ALVC162836
 20 Bit Universal Bus Driver with 3-STATE Outputs and 25Ω Resistors

Functional Comparison

The 74VCX162839 and 74ALVC162836 are pin and functionally equivalent for registered DIMM applications.

This means that one will see no functional difference when used in a registered DIMM application. There is however differences in the actual function of the devices. The 74VCX162839 was designed specifically for the Intel PC100 Rev 1.2 Registered DIMM specification and supports two modes of operation: a registered mode and a flow through mode. The 74ALVC162836 has additional functionality not required by the Intel PC100 Rev 1.2 Registered DIMM specification. While these devices support registered mode and flow through mode and flow through mode they have an additional latch mode.

When the devices are in registered or flow through mode they will behave as functional equivalents. The waveforms shown in Figure 3 show how the devices respond in flow through and registered modes.

The actual functional differences can only be seen by transitioning the REGE($\overline{\text{LE}}$) pin when the data latched into the internal register is different from the data on the input port. The waveforms to generate this condition are shown in Figure 4 (see pg.15). The 74VCX162839 is implemented such that the REGE pin selects between the flow through mode and the registered modes. The 74ALVC162836 is implemented such that the $\overline{\text{LE}}$ pin will force the internal latches enabled and pass data through these latches in flow through mode.

The functional differences shown do not impact registered DIMM Module application because the REGE pin is typically fixed in one state or the other for a given application. The implementation chosen for the 74VCX162839 was done to provide improved AC performance in flow-through mode.

unction Table for 7	4VCX162839
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	Inputs							
CLK	REGE	I _n	OE	0 _n				
↑	Н	Н	L	н				
↑	Н	L	L	L				
х	L	н	L	н				
х	L	L	L	L				
х	х	х	н	7				

H = Logic HIGH

L = Logic LOW

X = Don't Care, but not floating

F

Z = High Impedance

↑ = LOW-to-HIGH Transition

Connection I	Diagram for	74	VCX162839
		_	1
ŌĒ —	1	56	- CLK
°° —	2	55	— 'o
o ₁ —	3	54	— կ
GND —	4	53	— GND
0 ₂ —	5	52	— I ₂
o ₃ —	6	51	— I ₃
v _{cc} —	7	50	— v _{cc}
0 ₄ —	8	49	— I ₄
o ₅ —	9	48	— I ₅
0 ₆ —	10	47	— 1 ₆
GND —	11	46	- GND
0 ₇ —	12	45	— 1 ₇
° ₈ —	13	44	— I ₈
0 ₉ —	14	43	— I ₉
0 ₁₀ —	15	42	— I ₁₀
0 ₁₁ —	16	41	— I _{1.1}
0 ₁₂ —	17	40	- I ₁₂
GND —	18	39	— GND
0 ₁₃ —	19	38	— I ₁₃
0 ₁₄ —	20	37	— I ₁₄
0 ₁₅ —	21	36	— I ₁₅
v _{cc} —	22	35	— v _{cc}
0 ₁₆ —	23	34	— I ₁₆
0 ₁₇ —	24	33	— I ₁₇
GND —	25	32	- GND
0 _{1.8} —	26	31	— I ₁₈
0 ₁₉ —	27	30	— I ₁₉
NC —	28	29	- REGE

Logic Diagram for 74VCX162839



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Comparison of 74VCX162839 vs. 74ALVC162836 (Continued) Function Table for 74ALVC162836 Connection Diagram for 74ALVC162836

Г	Function Table for 74ALVC102050							
	Outputs							
OE	LE	CLK	A _n	Y _n				
н	Х	Х	х	Z				
L	L	Х	L	L				
L	L	Х	н	н				
L	н	\uparrow	L	L				
L	Н	↑	н	н				
L	н	L or H	х	Y ₀ (Note 8)				

Note 8: Output level before the indicated steady-state input conditions were established.

Jonnection	Diagramitor	74AI	_VC1020
[
ÕE —	1	48	-CLK
Y ₁ -	2	47	—A ₁
Y2-	3	46	— A ₂
GND —	4	45	— GND
Y ₃ —	5	44	— A ₃
Y ₄ —	6	43	— A ₄
v _{cc} –	7	42	— v _{cc}
Y ₅ -	8	41	— A ₅
Y ₆ —	9	40	— A _{.6}
gnd —	10	39	— GND
Y ₇ —	11	38	— A ₇
Y ₈ —	12	37	— A ₈
Y9 —	13	36	— A ₉
Y ₁₀ -	14	35	- A ₁₀
gnd —	15	34	— GND
Y ₁₁ -	16	33	—A ₁₁
Y ₁₂ —	17	32	-A ₁₂
v _{cc} –	18	31	— v _{cc}
Y ₁₃ —	19	30	-A ₁₃
Y ₁₄ —	20	29	— A ₁₄
gnd —	2 1	28	— GND
Y ₁₅ —	22	27	-A ₁₅
Y ₁₆ —	23	26	-A ₁₆
NC —	24	25	-LE

Logic Diagram for 74ALVC162836



Comparison of 74VCX162839 vs. 74ALVC162836 (Continued) AC Comparison

The following table shows a comparison of the 74VCX162839 device and the equivalent ALVC device. The table also compares performance vs. the Intel PC100 Rev 1.2 Registered DIMM specification.

AC Specifications Table

Parameter	Symbol	PC100 (1.2)		74VCX162839		74ALVC162836		11:40	Test Can ditions
		Min	Max	Min	Max	Min	Max	Units	Test Conditions
CLK Input Capacitance	C _{IN}	3.30	6.00	6.0	(Тур)	5.0	(Тур)	pF	10 MHz
Maximum Clock Frequency	f _{MAX}	150		250		150		MHz	
Output Edge Rate	t _{THL/LH}	1.00	2.50					V/ns	C _L = 50pF V _{CC} = 3.3V +/- 0.15V Between 1.2V -1.8V
Propagation Delay – Register	t _{PHL/LH} CLK to Y	1.9	4.5	1.1	4.7	1.1	5.0	ns	$C_{L} = 50 pF$ $V_{CC} = 3.3V +/- 0.15V$ CLK to any Y
Propagation Delay – Register	t _{PHL/LH} CLK to Y	1.4	2.9					ns	C _L = 0pF V _{CC} = 3.3V +/- 0.15V CLK to any Y
Propagation Delay – Buffer	t _{PHL/LH} A to Y	1.0	4.5	1.1	3.7	1.2	4.0	ns	$C_L = 50pF$ V _{CC} = 3.3V +/- 0.15V A to any Y
Propagation Delay – Buffer	t _{PHL/LH} A to Y	0.9	2.0					ns	C _L = 0pF V _{CC} = 3.3V +/- 0.15V A to any Y
Maximum Allowable SSO Delay			300					ps	C_L = 50pF, Any output combination, V _{CC} = 3.3V +/- 0.15V
Setup Time	t _{SET}	1.7		1.5		1.5		ns	V _{CC} = 3.3V +/- 0.15V Any input
Hold Time	t _{HOLD}	0.7		1.0		0.9		ns	V _{CC} = 3.3V +/- 0.15V Any input
Input Current	I _{IN}		10.0		5.0		5.0	uA	V _{IN} = 0V to 3.45V V _{CC} = 3.3V +/- 0.15V

Note: AC Specifications Table for the VCX and ALVC products above are for V_{CC} = \pm 10%, and T_A = -40 to 85°C

Conclusion

As can be seen from the above comparisons, Fairchild Semiconductor's solutions for buffered or registered DIMMs have comparable or better performance than competitive solutions. Through careful consideration of device performance, functional requirement, and bit-width requirements, successful PC100 DIMM designs can be achieved with high signal integrity and system performance.

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AN-5005 PC100 Memory Driver Competitive Comparisons