CS51033

Fast PFET Buck Controller Does Not Require Compensation

Description

The CS51033 is a switching controller for use in DC-DC converters. It can be used in the buck topology with a minimum number of external components. The CS51033 consists of a 1.0A power driver for controlling the gate of a discrete P-channel transistor, fixed frequency oscillator, short circuit protection timer, programmable soft start, precision reference, fast output voltage monitoring comparator, and output stage driver logic with latch.

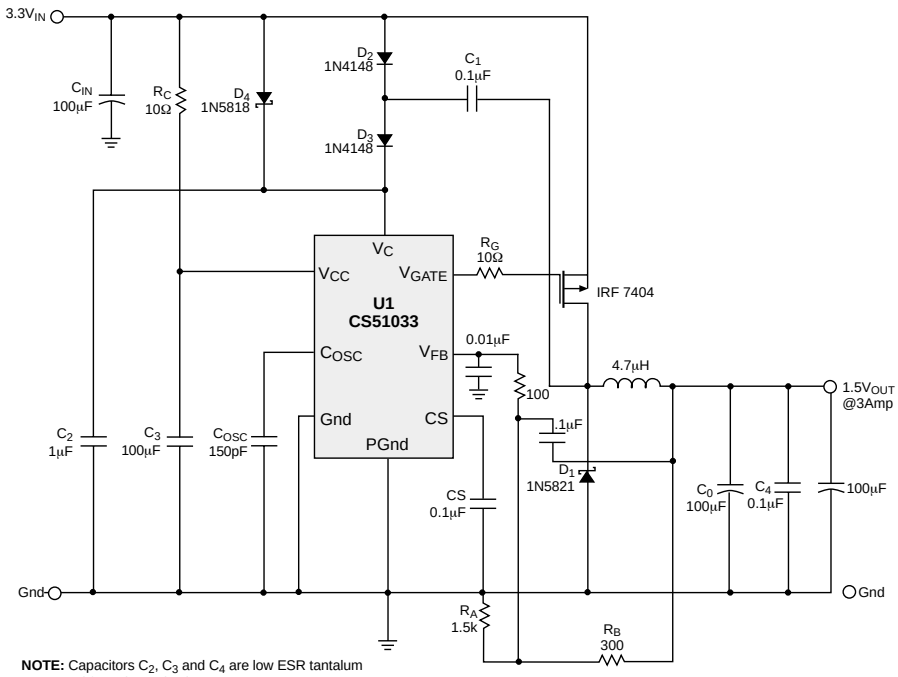
The high frequency oscillator allows the use of small inductors and output capacitors, minimizing PC board area and systems cost. The programmable soft start reduces current surges at start up. The short circuit protection timer significantly reduces the PFET duty cycle to approximately 1/30 of its normal cycle during short circuit conditions.

The CS51033 is available in 8L SO and 8L PDIP plastic packages.

Features

- 1A Totem Pole Output Driver
- High Speed Oscillator (700kHz max)
- No Stability Compensation Required
- Lossless Short Circuit Protection
- 2% Precision Reference
- Programmable Soft Start

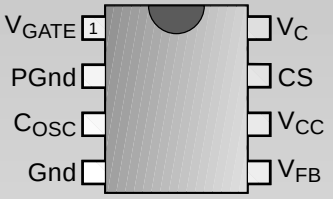
Typical Application Diagram



NOTE: Capacitors C_2, C_3 and C_4 are low ESR tantalum caps used for noise reduction.

Package Options

8 Lead SO Narrow & PDIP



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Absolute Maximum Ratings

Power Supply Voltage, V_{CC} 5V
Driver Supply Voltage, V_C 20V
Driver Output Voltage, V_{GATE} 20V
C_{OSC}, CS, V_{FB} (Logic Pins) 5V
Peak Output Current 1.0A
Steady State Output Current 200mA
Operating Junction Temperature, T_J ..... 150°C
Storage Temperature Range, T_S ..... -65 to 150°C
ESD (Human Body Model) 2kV
Lead Temperature Soldering
Wave Solder (through hole styles only) ..... 10 sec. max, 260°C peak
Reflow (SMD styles only) ..... 60 sec. max above 183°C, 230°C peak

Electrical Characteristics: Specifications apply for $3.135 \le V_{CC} \le 3.465V$, $3V \le V_C \le 16V$, $-40°C \le T_A \le 125°C$, $-40°C \le T_J \le 125°C$, unless otherwise specified.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ Oscillator	**V_{FB} = 1.2V**				
Frequency	C_{OSC} = 470pF	160	200	240	kHz
Charge Current	1.4V < V_{COSC} < 2V		110		µA
Discharge Current	2.7V > V_{COSC} > 2V		660		µA
Maximum Duty Cycle	$1 - (t_{OFF}/t_{ON})$	80.0	83.3		%
■ Short Circuit Timer	**V_{FB} = 1.0V; CS = 0.1µF; V_{COSC} = 2V**				
Charge Current	1V < V_{CS} < 2V	175	264	325	µA
Fast Discharge Current	2.55V > V_{CS} > 2.4V	40	66	80	µA
Slow Discharge Current	2.4V > V_{CS} > 1.5V	4	6	10	µA
Start Fault Inhibit Time		0.70	0.85	1.40	ms
Valid Fault Time	2.6V > V_{CS} > 2.4V	0.2	0.3	0.45	ms
GATE Inhibit Time	2.4V > V_{CS} > 1.5V	9	15	23	ms
Duty Cycle		2.5	3.1	4.6	%
■ CS Comparator	**V_{FB} = 1V**				
Fault Enable CS Voltage			2.5		V
Max. CS Voltage	V_{FB} = 1.5V		2.6		V
Fault Detect Voltage	V_{CS} when GATE goes high		2.4		V
Fault Inhibit Voltage	Minimum V_{CS}		1.5		V
Hold Off Release Voltage	V_{FB} = 0V	0.4	0.7	1.0	V
Regulator Threshold Voltage Clamp	V_{CS} = 1.5V	0.725	0.866	1.035	V
■ V_{FB} Comparator	**V_{COSC} = V_{CS} = 2V**				
Regulator Threshold Voltage	T_J = 25°C (Note 1) T_J = -40 to 125°C	1.225 1.210	1.250 1.250	1.275 1.290	V V
Fault Threshold Voltage	T_J = 25°C (Note 1) T_J = -40 to 125°C	1.12 1.10	1.15 1.15	1.17 1.19	V V
Threshold Line Regulation	$3.135V \le V_{CC} \le 3.465$		6	15	mV
Input Bias Current	V_{FB} = 0V		1	4	µA
Voltage Tracking	(Regulator Threshold Voltage - Fault Threshold Voltage)	70	100	120	mV
Input Hysteresis Voltage			4	20	mV

Electrical Characteristics: Specifications apply for $3.135 \le V_{CC} \le 3.465V$, $3V \le V_C \le 16V$, $-40°C \le T_J \le 125°C$, unless otherwise specified.					
PARAMETER	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
■ **Power Stage**	**$V_C = 10V$; $V_{FB} = 1.2V$**				
GATE DC Low Saturation Voltage	$V_{COSC} = 1V$; 200mA Sink		1.2	1.5	V
GATE DC High Saturation Voltage	$V_{COSC} = 2.7V$; 200mA Source; $V_C = V_{GATE}$		1.5	2.1	V
Rise Time	$C_{GATE} = 1nF$; $1.5V < V_{GATE} < 9V$		25	60	ns
Fall Time	$C_{GATE} = 1nF$; $9V > V_{GATE} > 1.5V$		25	60	ns
■ **Current Drain**					
I_{CC}	$3.135V < V_{CC} < 3.465V$, Gate switching		3.5	6.0	mA
I_C	$3V < V_C < 16V$, Gate non-switching		2.7	4.0	mA

Note1: Guaranteed by design not 100% tested in production.

Package Pin Description		
PACKAGE PIN #	**PIN SYMBOL**	**FUNCTION**
8L SO Narrow & PDIP		
1	V_{GATE}	Driver pin to gate of external PFET.
2	PGnd	Output power stage ground connection.
3	C_{OSC}	Oscillator frequency programming capacitor.
4	Gnd	Logic ground.
5	V_{FB}	Feedback voltage input.
6	V_{CC}	Logic supply voltage.
7	CS	Soft start and fault timing capacitor.
8	V_C	Driver supply voltage.

Block Diagram

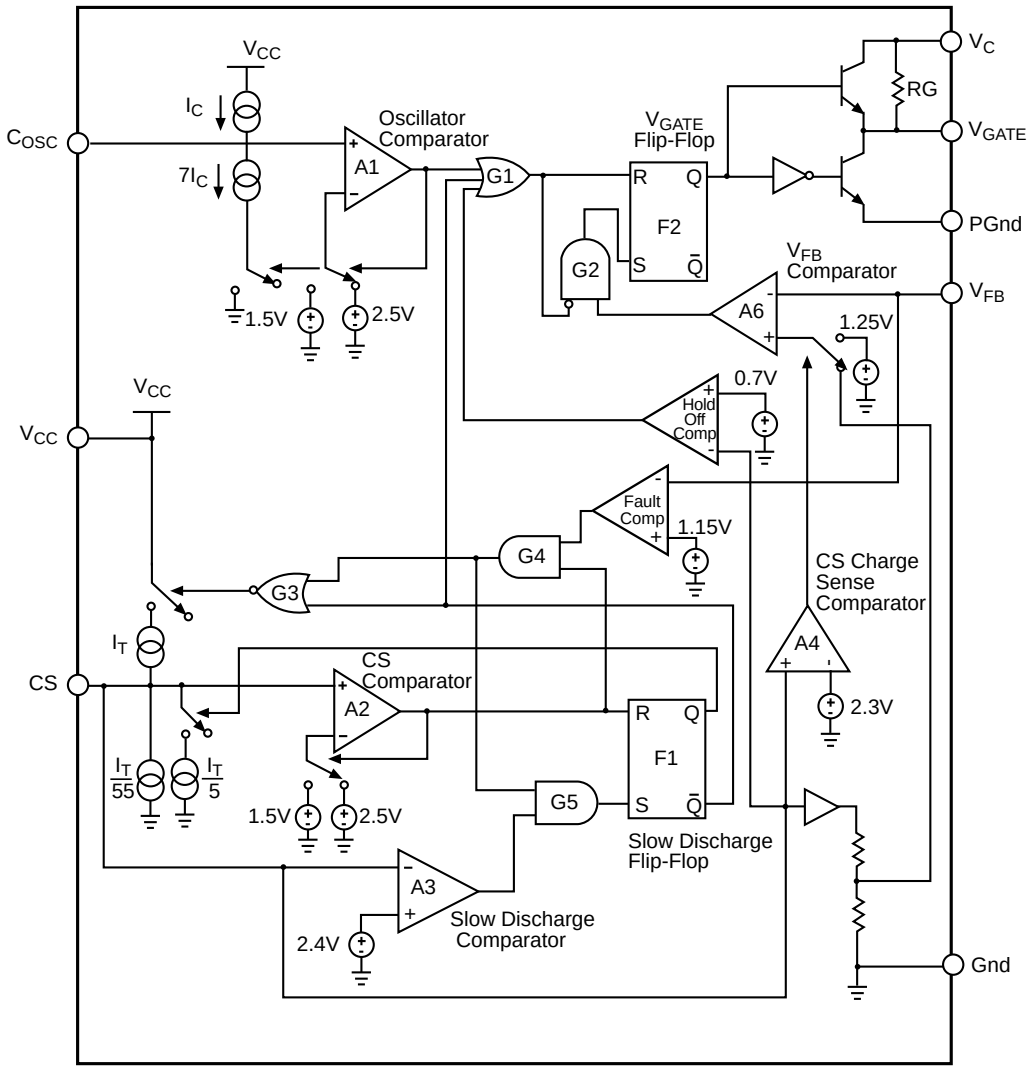


Figure 1: Block Diagram for CS51033

Circuit Description

Theory of Operation

Control Scheme

The CS51033 monitors the output voltage to determine when to turn on the PFET. If V_{FB} falls below the internal reference voltage of 1.25V during the oscillator's charge cycle, the PFET is turned on and remains on for the duration of the charge time. The PFET gets turned off and remains off during the oscillator's discharge cycle time with the maximum duty cycle to 80%. It requires 7mV typical, and 20mV maximum ripple on the V_{FB} pin is required to operate. This method of control does not require any loop stability compensation.

Startup

The CS51033 has an externally programmable soft start feature that allows the output voltage to come up slowly, preventing voltage overshoot on the output.

At startup, the voltage on all pins is zero. As V_{CC} rises, the V_C voltage along with the internal resistor R_G keeps the PFET off. As V_{CC} and V_C continue to rise, the oscillator capacitor (C_{OSC}) and the Soft start/Fault Timing capacitor (CS) charges via internal current sources. C_{OSC} gets charged by the current source I_C and CS gets charged by the I_T source combination described by:

$$I_{CS} = I_T - \left(\frac{I_T}{55} + \frac{I_T}{5} \right)$$

The internal Holdoff Comparator ensures that the external PFET is off until $V_{CS} > 0.7V$ preventing the GATE flip-flop (F2) from being set. This allows the oscillator to reach its operating frequency before enabling the drive output. Soft start is obtained by clamping the V_{FB} comparator's (A6) reference input to approximately 1/2 of the voltage at the CS pin during startup, permitting the control loop and the output voltage to slowly increase. Once the CS pin charges above the Holdoff Comparator trip point of 0.7V, the low

Circuit Description: continued

feedback to the V_{FB} Comparator sets the GATE flip-flop during C_{OSC} 's charge cycle. Once the GATE flip-flop is set, V_{GATE} goes low and turns on the PFET. When V_{CS} exceeds 2.4V, the CS charge sense comparator (A4) sets the V_{FB} comparator reference to 1.25V completing the startup cycle.

Lossless Short Circuit Protection

The CS51033 has "Lossless" short circuit protection since there is no current sense resistor required. When the voltage at the CS pin (the fault timing capacitor voltage) reaches 2.5V, the fault timing circuitry is enabled. During normal operation the CS voltage is 2.6V. During a short circuit condition or a transient condition, the output voltage moves lower and the voltage at V_{FB} drops. If V_{FB} drops below 1.15V, the output of the fault comparator goes high and the CS51033 goes into a fast discharge mode. The fault timing capacitor, CS, discharges to 2.4V. If the V_{FB} voltage is still below 1.15V when the CS pin reaches 2.4V, a valid fault condition has been detected. The slow discharge comparator output goes high and enables gate G5 which sets the slow discharge flip flop. The Vgate flip flop resets and the output switch is turned off. The fault timing capacitor is slowly discharged to 1.5V. The CS51033 then enters a normal startup routine. If the fault is still present when the fault timing capacitor voltage reaches 2.5V, the fast and slow discharge cycles repeat as shown in figure 2.

If the V_{FB} voltage is above 1.15V when CS reaches 2.4V a fault condition is not detected, normal operation resumes and CS charges back to 2.6V. This reduces the chance of erroneously detecting a load transient as a fault condition.

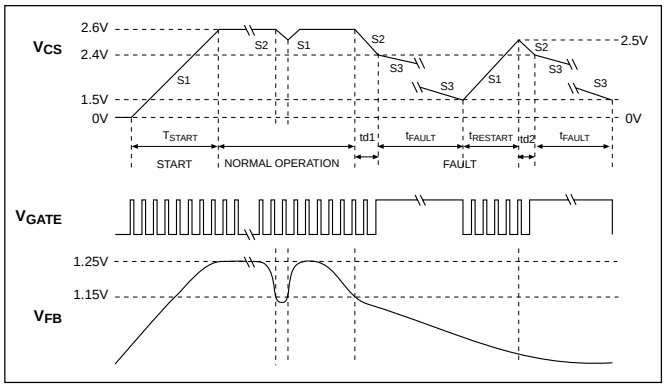


Figure 2. Voltage on start capacitor (V_{GS}), the gate (V_{GATE}), and in the feedback loop (V_{FB}), during startup, normal and fault conditions.

Buck Regulator Operation

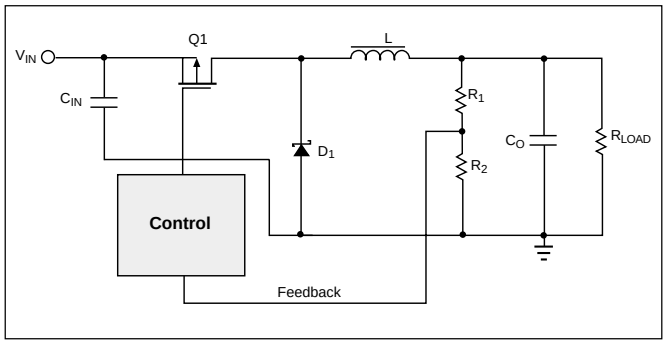


Figure 3. Buck regulator block diagram.

A block diagram of a typical buck regulator is shown in Figure 3. If we assume that the output transistor is initially off, and the system is in discontinuous operation, the inductor current I_L is zero and the output voltage is at its nominal value. The current drawn by the load is supplied by the output capacitor C_O . When the voltage across C_O drops below the threshold established by the feedback resistors R1 and R2 and the reference voltage V_{REF}, the power transistor Q1 switches on and current flows through the inductor to the output. The inductor current rises at a rate determined by $(V_{IN}-V_{OUT})/Load$. The duty cycle (or "on" time) for the CS51033 is limited to 80%. If the output voltage remains higher than nominal during the entire C_{OSC} charge time, the Q1 does not turn on, skipping the pulse.

CHARGE PUMP CIRCUIT

(Refer to the CS51033 Application Diagram)

An external charge pump circuit is necessary when the input voltage is below 5V to ensure that there is sufficient gate drive voltage for the external FET. When V_{IN} is applied, capacitors C1 and C2 will be charged to a diodes drop below V_{IN} via diodes D2 and D4, respectively. When the PFET turns on, its drain voltage will be approximately equal to V_{IN}. Since the voltage across C1 can not change instantaneously, D2 is reverse biased and the anode voltage rises to approximately 2*3.3V-VD2. C1 transfers some of its stored charge C2 via D3. After several cycles there is sufficient gate drive voltage.

Applications Information

Designing a Power Supply with the CS51033

Specifications

V_{IN} = 3.3V +/- 10% (i.e. 3.63V max., 2.97V min.)
V_{OUT} = 1.5V +/- 2%
I_{OUT} = 0.3A to 3A
Output ripple voltage < 33mV.
F_{SW} = 200kHz.

1) Duty Cycle Estimates

Since the maximum duty cycle, D, of the CS51033 is limited to 80% min. it is best to estimate the duty cycle for the various input conditions to see that the design will work over the complete operating range.
The duty cycle for a buck regulator operating in a continuous conduction mode is given by:

$$D = \frac{V_{OUT} + V_D}{V_{IN} - V_{SAT}}$$

Where V_{SAT} is Rdson × I_{OUT} Max.

In this case we can assume that V_D = 0.6V and V_{SAT} = 0.6V so the equation reduces to:

Applications Information: continued

$$D = \frac{V_{OUT}}{V_{IN}}$$

From this, the maximum duty cycle D_{MAX} is 53%, this occurs when V_{IN} is at its minimum while the minimum duty cycle D_{MIN} is 0.35%.

2) Switching Frequency and on and off time calculations.

F_{SW}= 200KHz. The switching frequency is determined by C_{OSC}, whose value is determined by :

$$C_{OSC} = \frac{95}{F_{sw} \times \left(1-\left(\frac{F_{SW}}{3 \times 10^{6}}\right)-\left(\frac{30 \times 10^{3}}{F_{SW}}\right)^{2}\right)} \cong 470pF$$

$$T = \frac{1}{F_{SW}} = 5\mu s$$

$$T_{ON(MAX)} = 5\mu s \times 0.53 = 2.65\mu s$$
$$T_{ON(MIN)} = 5\mu s \times 0.35 = 1.75\mu s$$
$$T_{OFF(MAX)} = 5\mu s - 0.7\mu s = 4.3\mu s$$

3) Inductor selection

Pick the inductor value to maintain continuous mode operation down to 0.3 Amps.

The ripple current $\Delta I = 2 \times I_{OUT(MIN)} = 2 \times 0.3A = 0.6A$.

$$L_{MIN} = \frac{V_{OUT} + V_D \times T_{OFF(MAX)}}{\Delta I} = \frac{2.1V \times 4.3\mu s}{0.6A} \cong 15\mu H$$

The CS51033 will operate with almost any value of inductor. With larger inductors the ripple current is reduced and the regulator will remain in a continuous conduction mode for lower values of load current. A smaller inductor will result in larger ripple current. The core must not saturate with the maximum expected current, here given by:

$$I_{MAX} = \frac{I_{OUT} + \Delta I}{2} = 3A + 0.6A/2 = 3.3A$$

4) Output Capacitor

The output capacitor limits the output ripple voltage. The CS51033 needs a maximum of 15mV of output ripple for the feedback comparator to change state. If we assume that all the inductor ripple current flows through the output capacitor and that it is an ideal capacitor (i.e. zero ESR), the minimum capacitance needed to limit the output ripple to 50mV peak to peak is given by:

$$C_O = \frac{\Delta I}{8 \times F_{SW} \times \Delta V} = \frac{0.6A}{8 \times (200 \times 10^{3}\,Hz) \times (33 \times 10^{-3}V)} \cong 11.4\mu F$$

The minimum ESR needed to limit the output voltage ripple to 50mV peak to peak is:

$$ESR = \frac{\Delta V}{\Delta I} = \frac{50 \times 10^{-3}}{0.6A} = 55m\Omega$$

The output capacitor should be chosen so that its ESR is at least half of the calculated value and the capacitance is at least ten times the calculated value. It is often advisable to use several capacitors in parallel to reduce the ESR.
Low impedance aluminum electrolytic, tantalum or organic semiconductor capacitors are a good choice for an output capacitor. Low impedance aluminum are the cheapest but are not available in surface mount at present. Solid tantalum chip capacitors are available from a number of suppliers and offer the best choice for surface mount applications. The capacitor working voltage should be greater than the output voltage in all cases.

5) V_{FB} Divider

$$V_{OUT} = 1.25V\left(\frac{R1 + R2}{R2}\right) = 1.25V\left(\frac{R1}{R2} + 1\right)$$

The input bias current to the comparator is 4μA. The resistor divider current should be considerably higher than this to ensure that there is sufficient bias current. If we choose the divider current to be at least 250 times the bias current this gives a divider current of 1mA and simplifies the calculations.

$$\frac{1.5V}{1mA} = R1+R2 = 1.5K\Omega$$

Let R2 = 1K

Rearranging the divider equation gives:

$$R1 = R2\left(\frac{V_{OUT}}{1.25} - 1\right) = 1K\Omega\left(\frac{1.5V}{1.25}\right) = 200\Omega$$

6) Divider bypass capacitor Crr

Since the feedback resistors divide the output voltage by a factor of 4, i.e. 5V/1.25V= 4 it follows that the output ripple is also divided by four. This would require that the output ripple be at least 60mV (4 × 15mV) to trip the feedback compactor. We use a capacitor Crr to act as an ac short so that the output ripple is not attenuated by the divider network. The ripple voltage frequency is equal to the switching frequency so we choose Crr so that:

$$X_C = \frac{1}{2\pi fC}$$

is negligible at the switching frequency.
In this case F_{SW} is 200kHz if we allow $X_C = 3\Omega$ then:

$$C = \frac{1}{2\pi f3} \cong 0.265\mu F$$

7) Soft start and Fault timing capacitor C_S.

C_S performs several important functions. First it provides a dead time for load transients so that the IC does not enter a fault mode every time the load changes abruptly. Secondly it disables the fault circuitry during startup, it also provides soft start by clamping the reference voltage during startup

to rise slowly and finally it controls the Hiccup short circuit protection circuitry. This function reduces the PFET's duty cycle to 2% of the C_S period.

The most important consideration in calculating C_S is that it's voltage does not reach 2.5V (the voltage at which the fault detect circuitry is enabled) before V_{FB} reaches 1.15V otherwise the power supply will never start.

If the V_{FB} pin reaches 1.15V the fault timing comparator will discharge C_S and the supply will not start. For the V_{FB} voltage to reach 1.15V the output voltage must be at least 4 × 1.15 = 4.6V.
If we choose an arbitrary startup time of 200μs we calculate the value of C_S from:

$$T = \frac{C_S \times 2.5V}{I_{CHARGE}}$$

$$C_{S(min)} = \frac{200\mu s \times 264\mu A}{2.5V} = 0.02\mu F$$

Use 0.1μf.

The fault time out time is the sum of the slow discharge time the fast discharge time and the recharge time and is obviously dominated by the slow discharge time.
The first parameter is the slow discharge time, it is the time for the C_S capacitor to discharge from 2.4V to 1.5V and is given by:

$$T_{SLOWDISCHARGE} = \frac{C_S \times (2.4V\text{-}1.5V)}{I_{DISCHARGE}}$$

Where $I_{DISCHARGE}$ is 6μA typical.

$$T_{SLOWDISCHARGE} = C_S \times 1.5V \times 10^5$$

The fast discharge time occurs when a fault is first detected. The C_S capacitor is discharged from 2.5V to 2.4V.

$$T_{FASTDISCHARGE} = \frac{C_S \times (2.5V - 2.4V)}{I_{FASTDISCHARGE}}$$

Where $I_{FASTDISCHARGE}$ is 66μA typical.

$$T_{FASTDISCHARGE} = C_S \times 1515$$

The recharge time is the time for C_S to charge from 1.5V to 2.5V.

$$T_{CHARGE} = \frac{C_S \times (2.5V\text{-}1.5V)}{I_{CHARGE}}$$

Where I_{CHARGE} is 264μA typical.

$$T_{CHARGE} = C_S \times 3787$$

The fault time out time is given by:

$$T_{FAULT} = C_S \times (3787 + 1515 + 1.5 \times 10^5)$$

$$T_{FAULT} = C_S \times 1.55 \times 10^5$$

For this circuit

$$T_{FAULT} = 0.1 \times 10^{-6} \times 1.55 \times 10^5 = 0.0155$$

A larger value of C_S will increase the fault time out time but will also increase the soft start time.

8) Input Capacitor.

The input capacitor reduces the peak currents drawn from the input supply and reduces the noise and ripple voltage on the V_{CC} and V_C pins. This capacitor must also ensure that the V_{CC} remains above the UVLO voltage in the event of an output short circuit. C_{IN} should be a low ESR capacitor of at least 100μf. A ceramic surface mount capacitor should also be connected between V_{CC} and ground to prevent spikes.

9) MOSFET Selection

The CS51033 drive a P-channel MOSFET. The V_{GATE} pin swings from Gnd to V_C. The type of PFET used depends on the operating conditions but for input voltages below 7V a logic level FET should be used.
Choose a PFET with a continuous drain current (Id) rating greater than the maximum output current. $R_{DS(on)}$ should be less than

$$R_{DS} <= \frac{0.6V}{I_{OUT(max)}} 167m\Omega$$

The Gate-to-Source voltage VGS and the Drain-to Source Breakdown Voltage should be chosen based on the input supply voltage.

The power dissipation due to the conduction losses is given by:

$$P_D = {}_{OUT}{}^2 \times R_{DS(on)} \times D$$

The power dissipation due to the switching losses is given by:

$$P_D = 0.5 \times V_{IN} \times I_{OUT} \times (T_R{}^r + T_F) \times F_{SW}$$

Where tr =Rise Time and tf= Fall Time.

10) Diode Selection.

The flyback or catch diode should be a Schottky diode because of it's fast switching ability and low forward voltage drop. The current rating must be at least equal to the maximum output current. The breakdown voltage should be at least 20V for this 12V application.
The diode power dissipation is given by:

$$P_D = I_{OUT} \times V_D \times (1\text{-}D_{MIN})$$

Package Specification

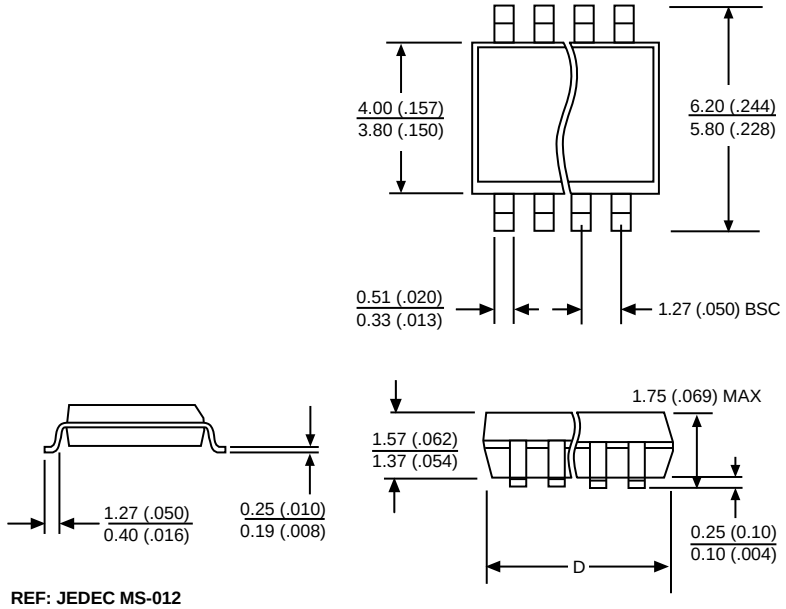
PACKAGE DIMENSIONS IN mm (INCHES)

Lead Count	D			
	Metric		English	
	Max	Min	Max	Min
8L SO Narrow	5.00	4.80	.197	.189
8L PDIP	10.16	9.02	.400	.355

PACKAGE THERMAL DATA

Thermal Data		8L SO Narrow	8L PDIP	
$R_{\Theta JC}$	typ	45	52	°C/W
$R_{\Theta JA}$	typ	165	100	°C/W

Surface Mount Narrow Body (D); 150 mil wide



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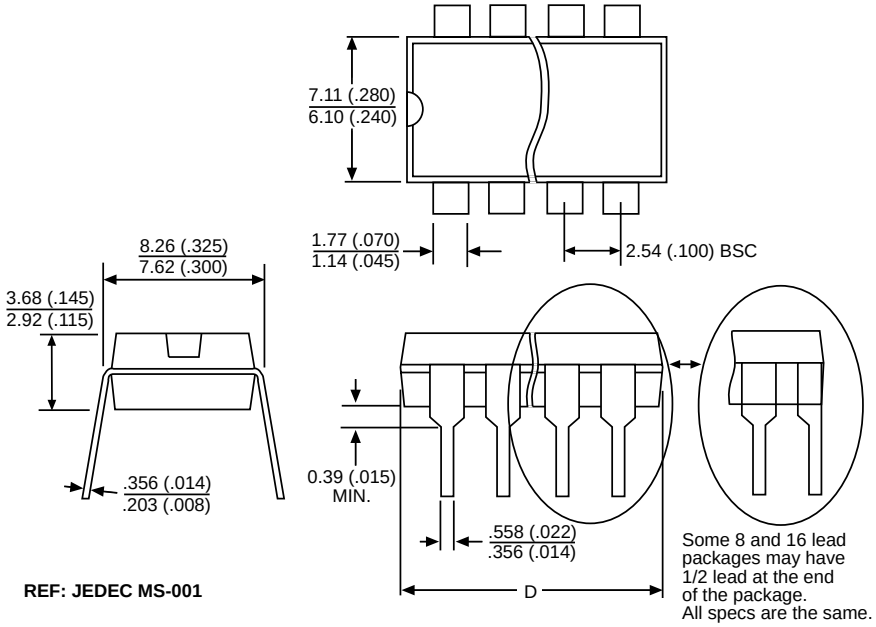
Plastic DIP (N); 300 mil wide



REF: JEDEC MS-001

Ordering Information

Part Number	Description
CS51033YD8	8L SO Narrow
CS51033YDR8	8L SO Narrow *(tape & reel)*
CS51033YN8	8L PDIP

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