Dual Low Offset, Low Power Operational Amplifier

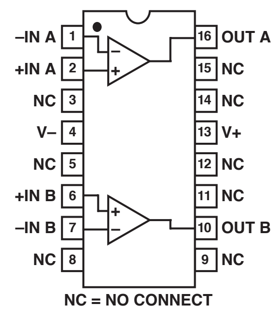
OP200

FEATURES

- Low Input Offset Voltage: 75 µV Max
- Low Offset Voltage Drift, Over –55°C ≤ T_A ≤ +125°C: 0.5 µV/°C Max
- Low Supply Current (Per Amplifier): 725 µA Max
- High Open-Loop Gain: 5000 V/mV Min
- Low Input Bias Current: 2 nA Max
- Low Noise Voltage Density: 11 nV/$\sqrt{Hz}$ at 1 kHz
- Stable with Large Capacitive Loads: 10 nF Typ
- Pin Compatible to OP221, MC1458, and LT1013 with Improved Performance
- Available in Die Form

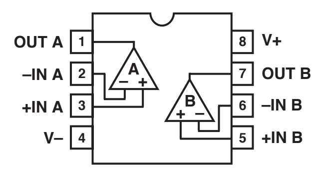
PIN CONNECTIONS

16-Pin SOIC (S-Suffix)



EPOXY MINI-DIP (P-Suffix),

8-Pin Hermetic DIP (Z-Suffix)



GENERAL DESCRIPTION

The OP200 is the first monolithic dual operational amplifier to offer OP77 type precision performance. Available in the industry standard 8-pin pinout, the OP200 combines precision performance with the space and cost savings offered by a dual amplifier.

The OP200 features an extremely low input offset voltage of less than 75 µV with a drift below 0.5 µV/°C, guaranteed over the full military temperature range. Open-loop gain of the OP200 exceeds 5,000,000 into a 10 kΩ load; input bias current is under 2 nA; CMR is over 120 dB and PSRR below 1.8 µV/V. On-chip zener-zap trimming is used to achieve the extremely low input offset voltage of the OP200 and eliminates the need for offset pulling.

Power consumption of the OP200 is very low, with each amplifier drawing less than 725 µA of supply current. The total current drawn by the dual OP200 is less than one-half that of a single OP07, yet the OP200 offers significant improvements over this industry standard op amp. The voltage noise density of the OP200, 11 nV/$\sqrt{Hz}$ at 1 kHz, is half that of most competitive devices.

The OP200 is pin compatible with the OP221, LM158, MC1458/1558, and LT1013.

The OP200 is an ideal choice for applications requiring multiple precision op amps and where low power consumption is critical.

For a quad precision op amp, see the OP400.

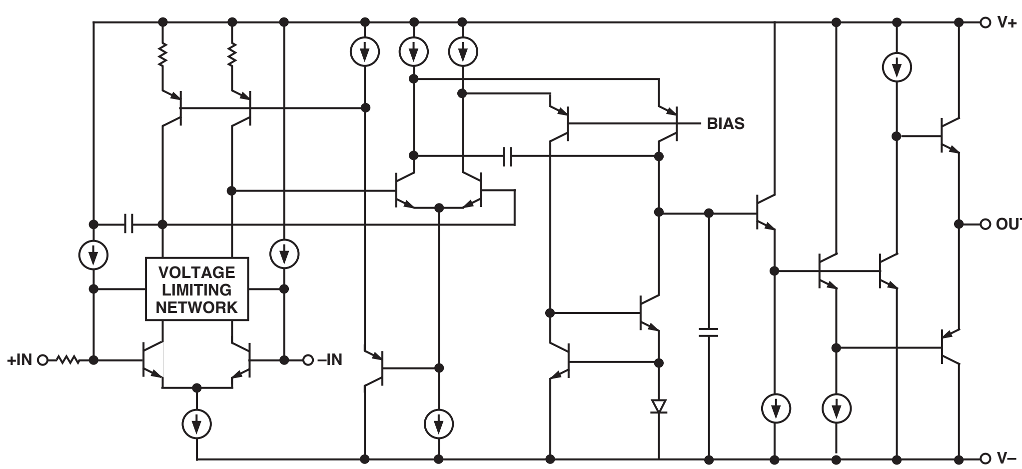


Figure 1. Simplified Schematic (One of two amplifiers is shown.)

REV. A

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OP200–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15$ V, $T_A = 25°C$, unless otherwise noted.)

Parameter	Symbol	Conditions	OP200A/E Min	OP200A/E Typ	OP200A/E Max	OP200F Min	OP200F Typ	OP200F Max	OP200G Min	OP200G Typ	OP200G Max	Unit
Input Offset Voltage	V_{OS}			25	75		50	150		80	200	µV
Long Term Input Voltage Stability				0.1			0.1			0.1		µV/mo
Input Offset Current	I_{OS}	$V_{CM} = 0$ V		0.05	1.0		0.05	2.0		0.05	3.5	nA
Input Bias Current	I_B	$V_{CM} = 0$ V		0.1	2.0		0.1	4.0		0.1	5.0	nA
Input Noise Voltage	$e_{n\ p\text{-}p}$	0.1 Hz to 10 Hz		0.5			0.5			0.5		$\mu V_{p\text{-}p}$
Input Noise Voltage Density[1]	e_n	$f_O = 10$ Hz $f_O = 1000$ Hz		22 11	36 18		22 11	36 18		22 11		$nV/\sqrt{Hz}$
Input Noise Current	$i_{n\ p\text{-}p}$	0.1 Hz to 10 Hz		15			15			15		$pA_{p\text{-}p}$
Input Noise Current Density	i_n	$f_O = 10$ Hz		0.4			0.4			0.4		$pA/\sqrt{Hz}$
Input Resistance Differential Mode	R_{IN}			10			10			10		MΩ
Input Resistance Common Mode	R_{INCM}			125			125			125		GΩ
Large Signal Voltage Gain	A_{VO}	V_O - ±10 V $R_L = 10$ kΩ $R_L = 2$ kΩ	 5000 2000	 12000 3700		 3000 1500	 7000 3200		 3000 1500	 7000 3200		M/mV

NOTES
[1]Sample tested
[2]Guaranteed but not 100% tested
[3]Guaranteed by CMR test

ELECTRICAL CHARACTERISTICS (V_S = 15 V, –55°C ≤ T_A ≤ +125°C for OP200A, unless otherwise noted.)

Parameter	Symbol	Conditions	OP200A Min	OP200A Typ	OP200A Max	Unit
Input Offset Voltage	V_{OS}			45	125	µV
Average Input Offset Voltage Drift	TCV_{OS}			0.2	0.5	µV/°C
Input Offset Current	I_{OS}	VCM = 0 V		0.15	2.5	nA
Input Bias Current	I_B	VCM = 0 V		0.9	5.0	nA
Large Signal Voltage Gain	A_{VO}	V_O = 10 V R_L = 10 Ω R_L = 2 kΩ	 3000 1000	 9000 2700		 V/mV V/mV
Input Voltage Range*	IVR		±12	±12.5		V
Common-Mode Rejection	CMR	V_{CM} = ±12 V	115	130		dB
Power Supply Rejection Ratio	PSRR	V_S = +3 V to +18 V		0.2	3.2	µV/V
Output Voltage Swing	V_O	R_L = 10 kΩ R_L = 2 kΩ	±12 ±11	±12.4 ±12		V V
Supply Current Per Amplifier	I_{SY}	No Load		600	775	µA
Capacitive Load Stability		A_V = +1		8		nF

NOTE
*Guaranteed by CMR test.

ELECTRICAL CHARACTERISTICS (V_S = ±15 V, T_A = 25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	OP200A/E Min	OP200A/E Typ	OP200A/E Max	OP200F Min	OP200F Typ	OP200F Max	OP200G Min	OP200G Typ	OP200G Max	Unit
Input Voltage Range[3]	IVR		±12	±13		±12	±13		±12	±13		V
Common-Mode Rejection	CMR	V_{CM} = ±12 V	120	135		115	135		110	130		dB
Power Supply Rejection Ratio	PSRR	V_S = ±3 V to ±18 V		0.4	1.8		0.4	3.2		0.6	5.6	µV/V
Output Voltage Swing	V_O	R_L= 10 kΩ R_L = 2 kΩ	±12 ±11	±12.6 ±12.2		±12 ±11	±12.6 ±12.2		±12 ±11	±12.6 ±12.2		V V
Supply Current Per Amplifier	I_{SY}	No Load		570	725		570	725		570	725	µA
Slew Rate	SR		0.1	0.15		0.1	0.15		0.1	0.15		V/µS
Gain Bandwidth Product	GBWP	A_V = 1		500			500			500		kHz
Channel Separation[2]	CS	V_O = 20 Vp-p f_O = 10 Hz	123	145		123	145		123	145		dB
Input Capacitance	C_{IN}			3.2			3.2			3.2		pF
Capacitive Load Stability		A_V = 1 No Oscillations		10			10			10		nF

NOTES
[1]Sample tested
[2]Guaranteed but not 100% tested
[3]Guaranteed by CMR test

OP200–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (V_S = ±15 V, –40°C ≤ T_A ≤ +85°C, unless otherwise noted.)

Parameter	Symbol	Conditions	OP200E Min	OP200E Typ	OP200E Max	OP200F Min	OP200F Typ	OP200F Max	OP200G Min	OP200G Typ	OP200G Max	Unit
Input Offset Voltage	V_{OS}			35	100		80	250		110	300	µV
Average Input Offset Voltage Drift	TCV_{OS}			0.2	0.5		0.5	1.5		0.6	2.0	µV/°C
Input Offset Current	I_{OS}	V_{CM} = 0 V		0.08	2.5		0.08	3.5		0.1	6.0	nA
Input Bias Current	I_B	V_{CM} = 0 V		0 3	5.0		0.3	70		0.5	10.0	nA
Large-Signal Voltage Gain	A_{VO}	V_O = ±10 V R_L= 10 kΩ R_L = 2 kΩ	3000 1500	10000 3200		2000 1000	5000 2500		2000 1000	5000 2500		V/mV V/mV
Input Voltage Range*	IVR		±12	±12.5		±12	±12.5		±12	±12.5		V
Common-Mode Rejection	CMR	V_{CM} = ±12 V	115	130		110	130		105	130		dB
Power Supply Rejection Ratio	PSRR	V_S = ±3 V to ±18 V		0.15	3.2		0.15	5.6		0.3	10.0	µV/V
Output Voltage Swing	V_O	R_L = 10 kΩ R_L = 2 kΩ	±12 ±11	±12.4 ±12		±12 ±11	±12.4 ±12		±12 ±11	±12.4 ±12.2		V V
Supply Current Per Amplifier	I_{SY}	No Load		600	775		600	775		600	775	µA
Capacitive Load Stability		A_V = 1 No Oscillations		10 10			10 10			10 10		nF nF

NOTE
*Guaranteed by CMR test.

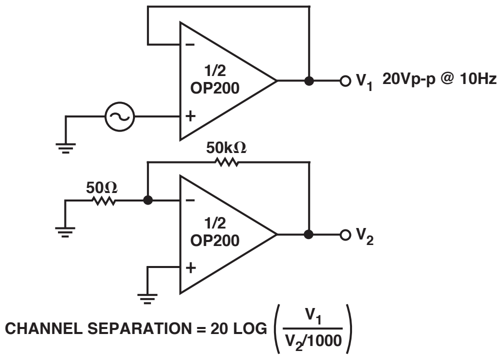


Figure 2. Channel Separation Test Circuit

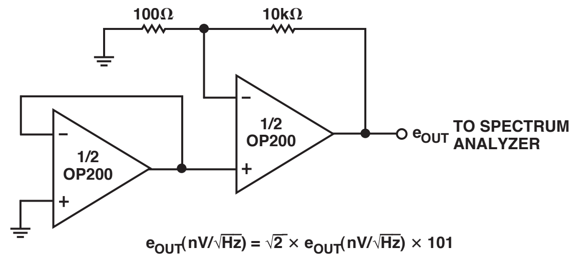


Figure 3. Noise Test Schematic

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . ±20 V
Differential Input Voltage . . . . ±30 V
Input Voltage . . . . Supply Voltage
Output Short-Circuit Duration . . . . Continuous
Storage Temperature Range
  P, S, Z-Package . . . . –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . 300°C
Junction Temperature (T_J) . . . . –65°C to +150°C
Operating Temperature Range
  OP200A . . . . –55°C to +125°C
  OP200E, OP200F . . . . –40°C to +85°C
  OP200G . . . . –40°C to +85°C

Package Type	θ_{JA}[2]	θ_{JC}	Unit
8-Pin Hermetic DIP (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	96	37	°C/W
16-Pin SOL (S)	92	27	°C/W

NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for CERDIP and P-DIP packages; θ_{JA} is specified for device soldered to printed circuit board for SOL package.

ORDERING GUIDE

	Package		
T_A = 25°C V_{OS} Max (μV)	CERDIP 8-Pin	Plastic	Operating Temperature Range
75	OP200AZ		MIL
75	OP200EZ		XIND
150	OP200FZ*		XIND
200		OP200GP	XIND
200		OP200GS	XIND

*Not for new design, obsolete April 2002.

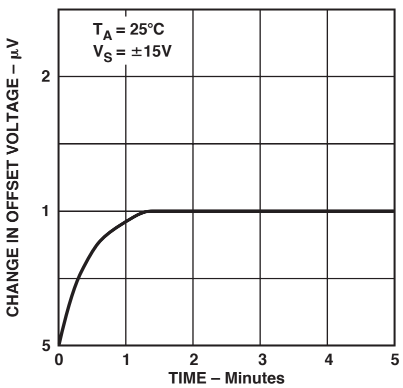
For military processed devices, please refer to the Standard Microcircuit Drawing (SMD) available at www.dscc.dla.mil/programs/milspec/default.asp

SMD Part Number	ADI Equivalent
5962-8859301M2A	OP200ARCMDA
5962-8859301MPA	OP200AZMDA

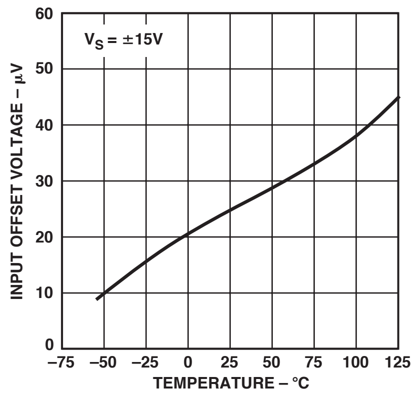
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the OP200 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

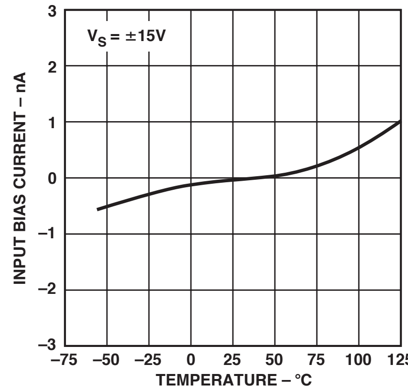
OP200–Typical Performance Characteristics



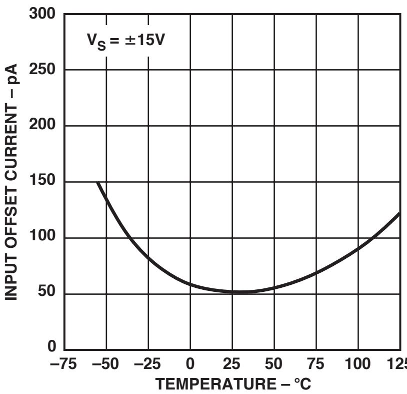
TPC 1. *Warm-Up Drift*



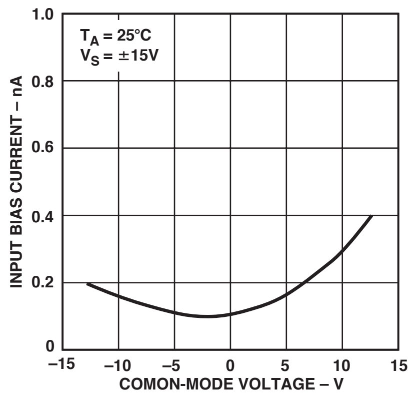
TPC 2. *Input Offset Voltage vs. Temperature*



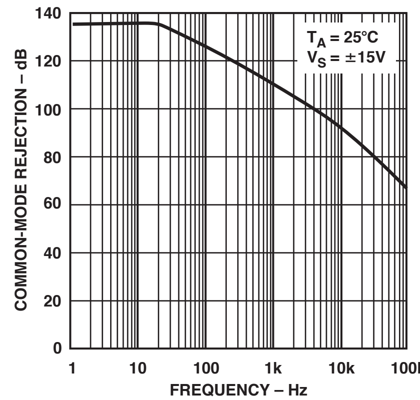
TPC 3. *Input Bias Current vs. Temperature*



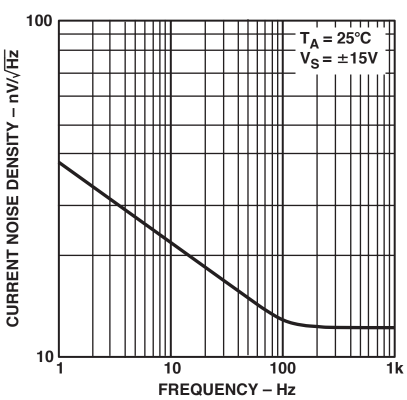
TPC 4. *Input Offset Current vs. Temperature*



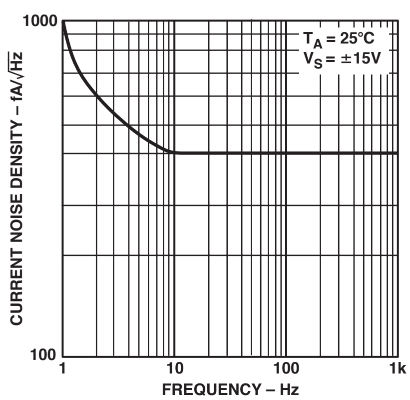
TPC 5. *Input Bias Current vs. Common-Mode Voltage*



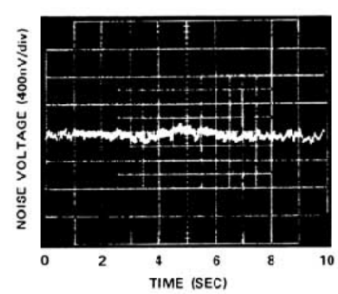
TPC 6. *Common-Mode Rejection vs. Frequency*



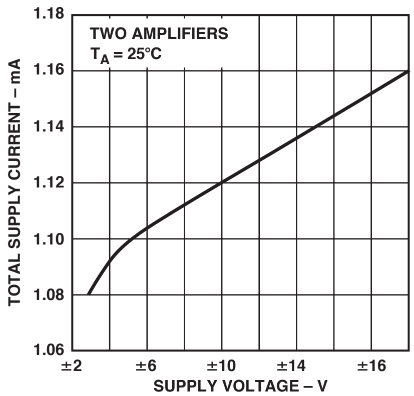
TPC 7. *Voltage Noise Density vs. Frequency*



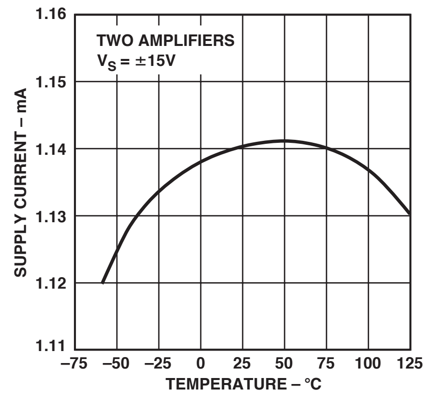
TPC 8. *Current Noise Density vs. Frequency*



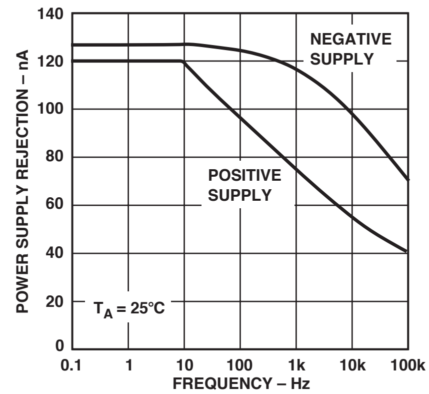
TPC 9. *0.1 to 10Hz Noise*



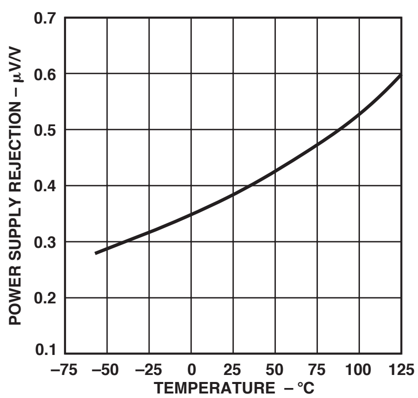
TPC 10. Total Supply Current vs. Supply Voltage



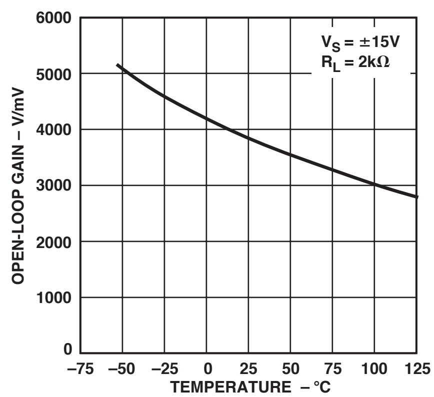
TPC 11. Total Supply Current vs. Temperature



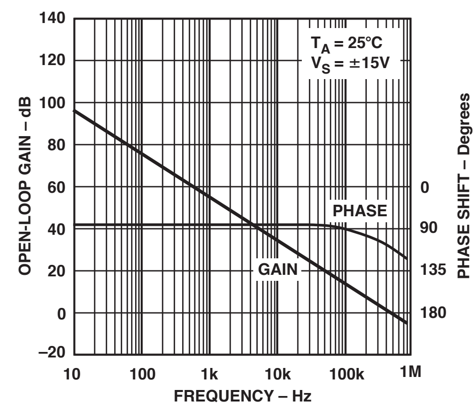
TPC 12. Power Supply Rejection vs. Temperature



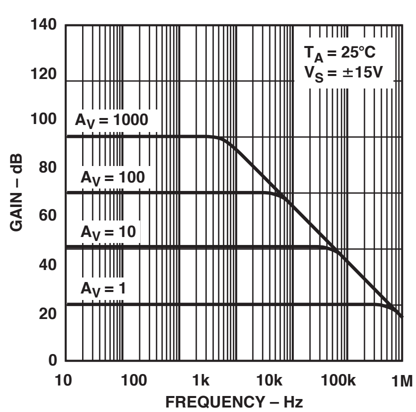
TPC 13. Power Supply Rejection vs. Temperature



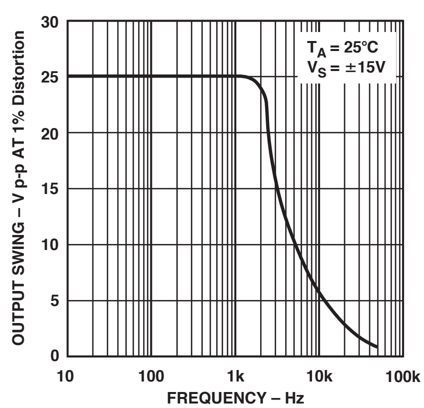
TPC 14. Open Loop Gain vs. Temperature



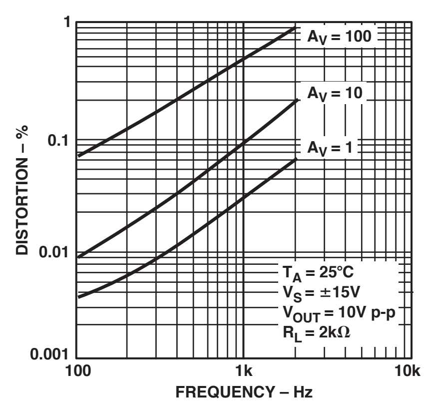
TPC 15. Open Loop Gain and Phase Shift vs. Frequency



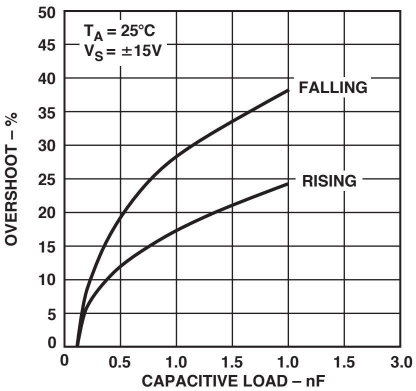
TPC 16. Closed Loop Gain vs. Frequency



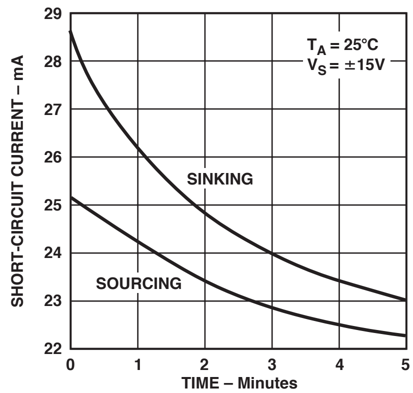
TPC 17. Maximum Output Swing vs. Frequency



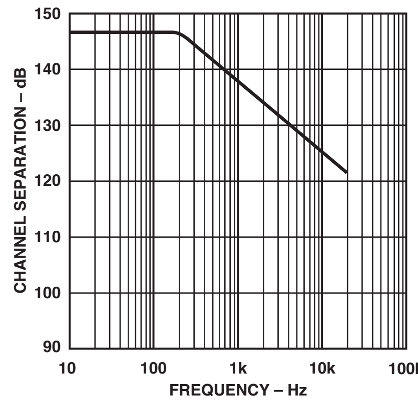
TPC 18. Total Harmonic Distortion vs. Frequency



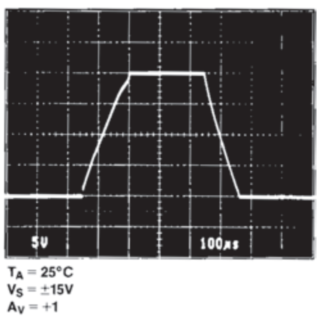
TPC 19. Overshoot vs. Capacitive Load



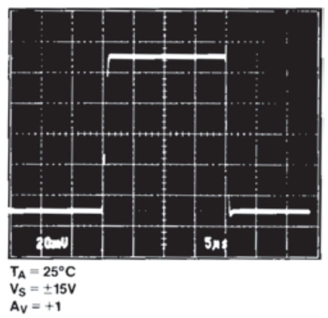
TPC 20. Short-Circuit Current vs. Time



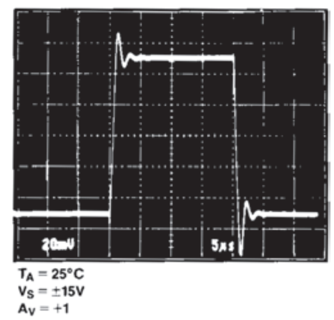
TPC 21. Channel Separation vs. Frequency



TPC 22. Large-Signal Transient Response



TPC 23. Small-Signal Transient Response



TPC 24. Small-Signal Transient Response C_{LOAD} = 1 nF

APPLICATIONS INFORMATION

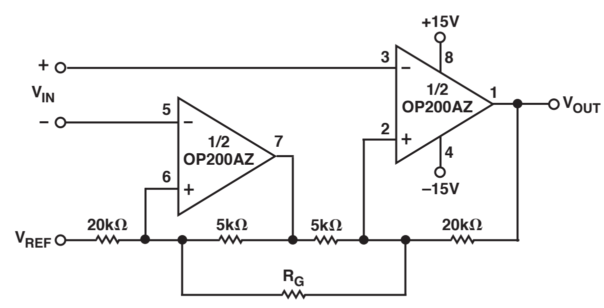
The OP200 is inherently stable at all gains and is capable of driving large capacitive loads without oscillating. Nonetheless, good supply decoupling is highly recommended. Proper supply decoupling reduces problems caused by supply line noise and improves the capacitive load driving capability of the OP200.

APPLICATIONS

DUAL LOW-POWER INSTRUMENTATION AMPLIFIER

A dual instrumentation amplifier that consumes less than 33 mW of power per channel is shown in Figure 4. The linearity of the instrumentation amplifier exceeds 16 bits in gains of 5 to 200 and is better than 14 bits in gains from 200 to 1000. CMRR is above 115 dB (Gain = 1000). Offset voltage drift is typically 0.2 μV/°C over the military temperature range which is comparable to the best monolithic instrumentation amplifiers. The bandwidth of the low-power instrumentation amplifier is a function of gain and is shown below:

Gain	Bandwidth
5	150 kHz
10	67 kHz
100	7.5 kHz
1000	500 Hz



$$V_{OUT} = \left(5 + \frac{40000}{R_G}\right) V_{IN} + V_{REF}$$

Figure 4. Dual Low-Power Instrumentation Amplifier

The output signal is specified with respect to the reference input, which is normally connected to analog ground. The reference input can be used to offset the output from –10 V to +10 V if required.

PRECISION ABSOLUTE VALUE AMPLIFIER

The circuit of Figure 5 is a precision absolute value amplifier with an input impedance of 10 MΩ. The high gain and low TCV_{OS} of the OP200 ensure accurate operation with microvolt input signals. In this circuit, the input always appears as a common-mode signal to the op amps. The CMR of the OP200 exceeds 120 dB, yielding an error of less than 2 ppm.

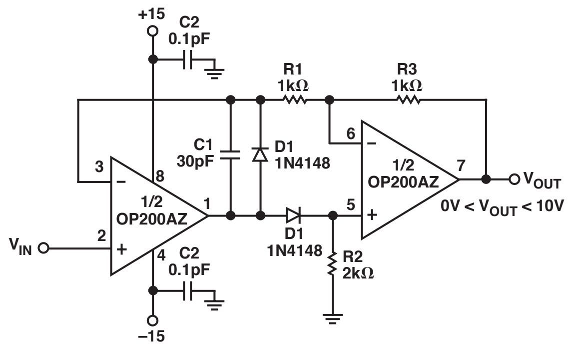


Figure 5. Precision Absolute Value Amplifier

PRECISION CURRENT PUMP

Maximum output current of the precision current pump shown in Figure 6 is ±10 mA. Voltage compliance is ±10 V with ±15 V supplies. Output impedance of the current transmitter exceeds 3 MΩ with linearity better than 16 bits.

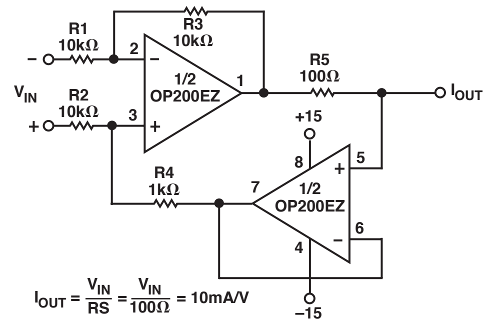


Figure 6. Precision Current Pump

DUAL 12-BIT VOLTAGE OUTPUT DAC

The dual output DAC shown in Figure 7 is capable of providing untrimmed 12-bit accurate operation over the entire military temperature range. Offset voltage, bias current and gain errors of the OP-200 contribute less than 1/lO of an LSB error at 12 bits over the military temperature range.

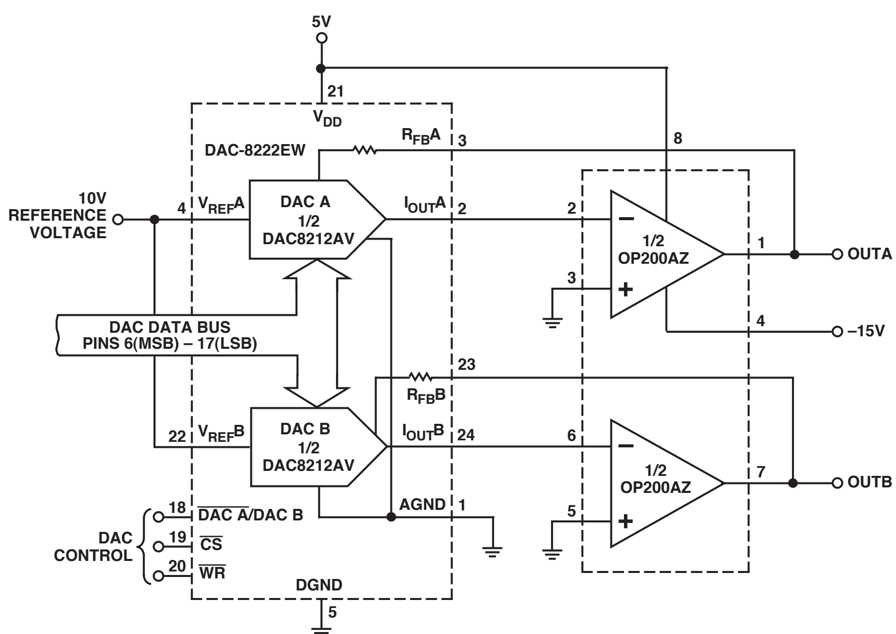


Figure 7. Dual 12-Bit Voltage Output DAC

DUAL PRECISION VOLTAGE REFERENCE

A dual OP200 and a REF-43, a 2.5 V reference, can be used to build a ±2.5 V precision voltage reference. Maximum output current from each reference is ±10 mA with load regulation under 25 µV/mA. Line regulation is better than 15 µV/V and output voltage drift is under 20 µV/°C. Output voltage noise from 0.1 Hz to 10 Hz is typically 75 µV p-p. R1 and D1 ensure correct start-up.

PROGRAMMABLE HIGH RESOLUTION WINDOW COMPARATOR

The programmable window comparator shown in Figure 9 is easily capable of 12-bit accuracy over the full military temperature range. A dual CMOS 12-bit DAC, the DAC-8212, is used in the voltage switching mode to set the upper and lower thresholds (DAC A and DAC B, respectively).

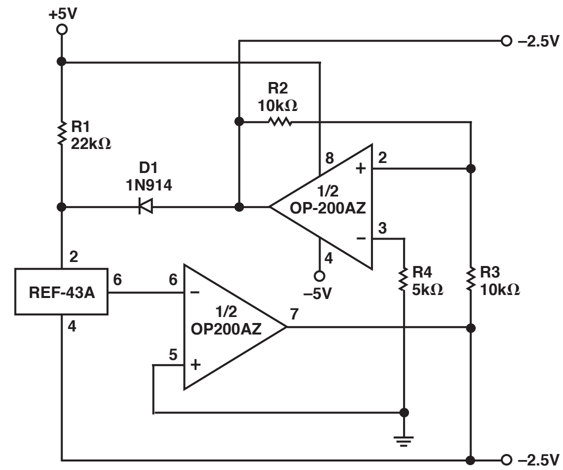


Figure 8. Dual Precision Voltage Reference

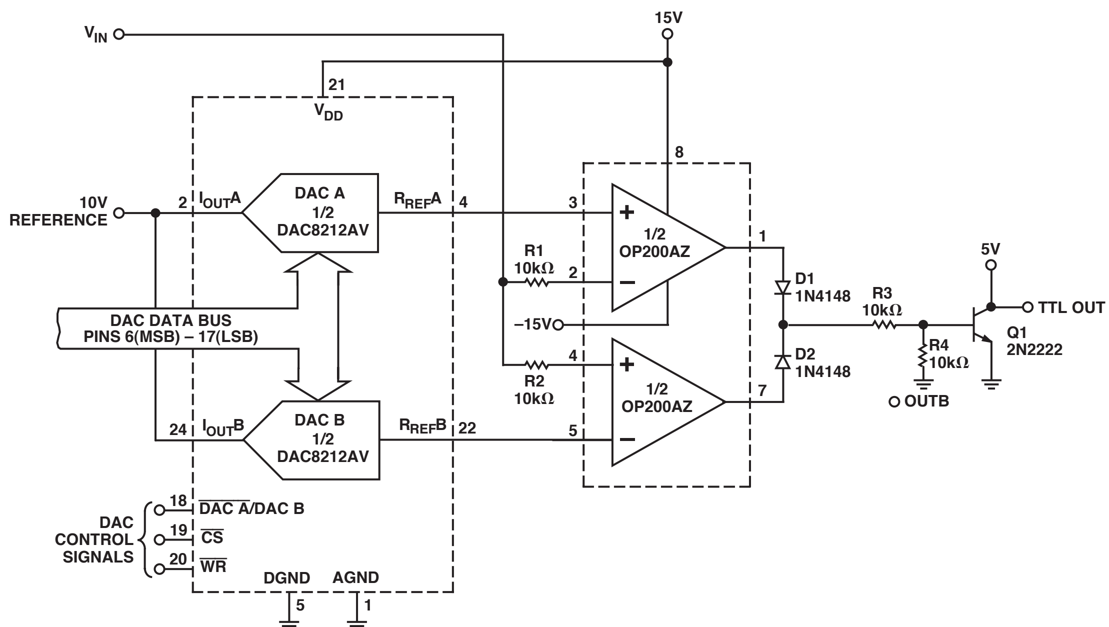


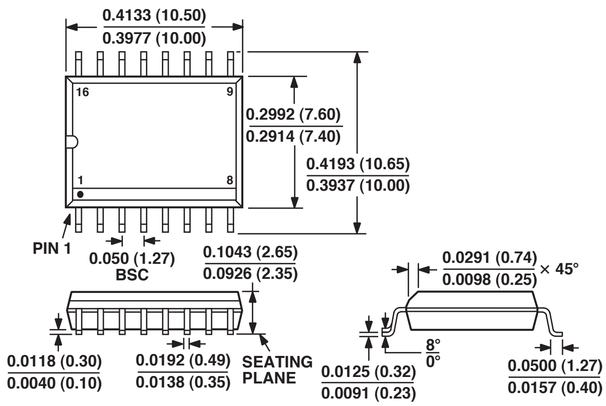
Figure 9. Programmable High Resolution Window Comparator

OUTLINE DIMENSIONS

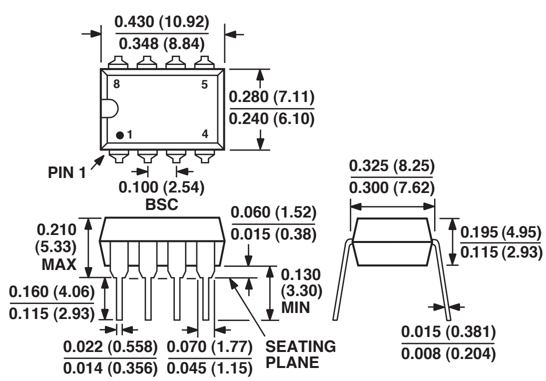
Dimensions shown in inches and (mm).

PIN CONNECTIONS

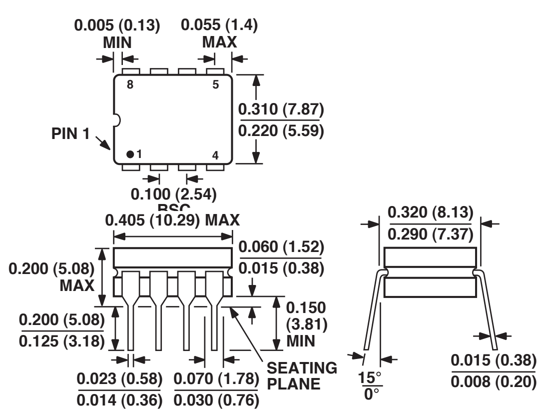
16-Pin SOIC (S-Suffix)



Epoxy MINI-DIP (P-Suffix)



8-Pin Hermetic DIP (Z-Suffix)



Revision History

C00322–0–4/02(A)

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